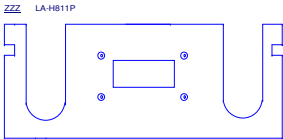


MODEL NAME : *Modena*  
PCB NO : *LA-H811P*  
BOM P/N : *451AHT31L01 ~ L32*



# Dell/Compal Confidential

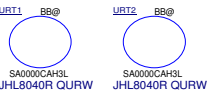
## Schematic Document

### (MODENA ICE Lake U)

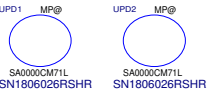
#### CPU Option



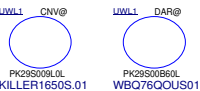
#### TBT Option



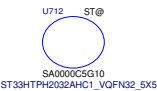
#### PD Option



#### WLAN Option



#### TPM Option

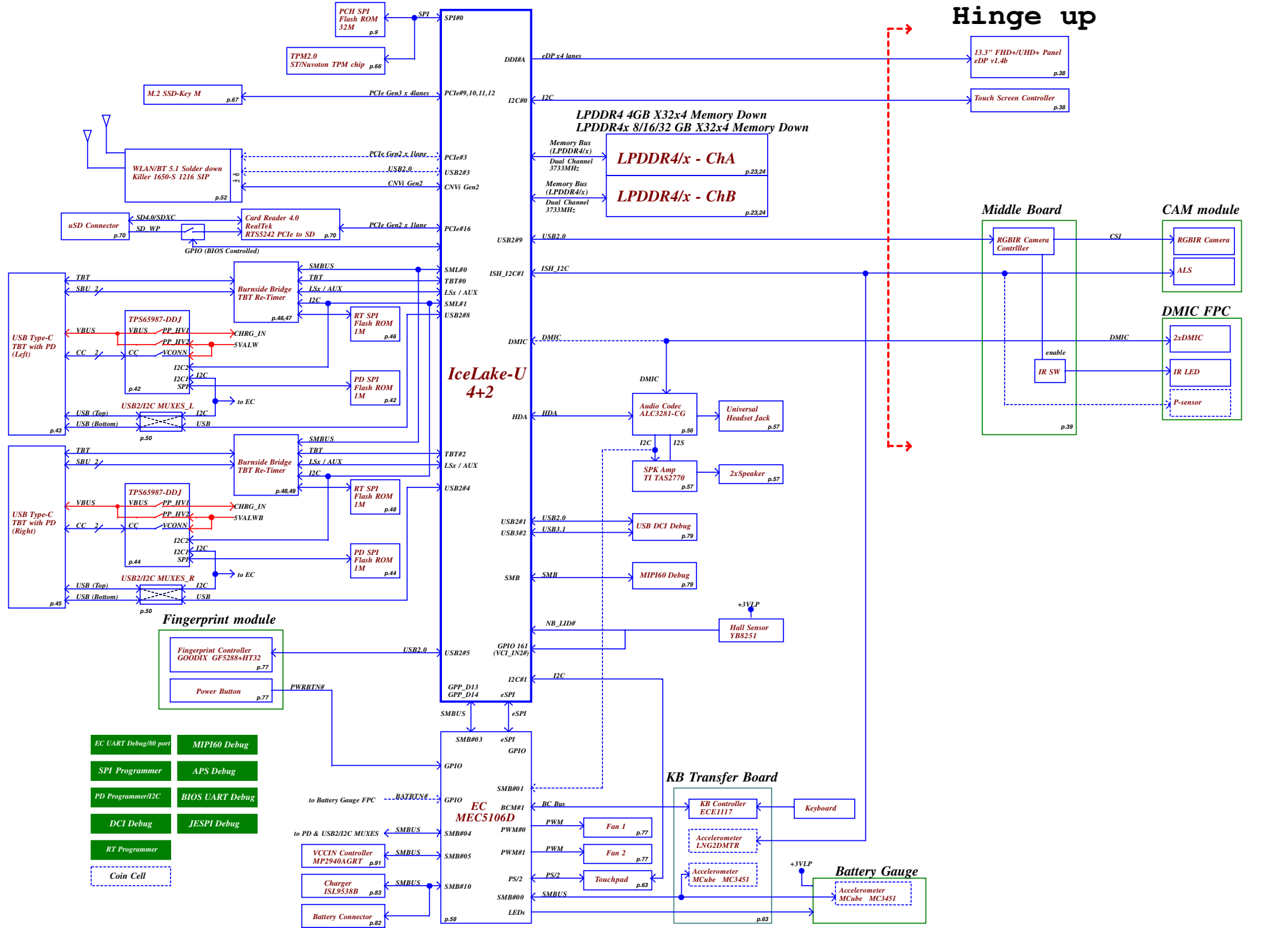


#### EC Option



2019-12-16  
Rev: 1.0 (A00)

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Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	PCB Revision
0	240K +/- 1%	4700p	X00	0.1
1	130K +/- 5%	4700p	X01	0.2
2	62K +/- 5%	4700p	X02	0.3
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	1K +/- 5%	4700p	N/A	N/A

SMBUS Control Table

	SOURCE	PCH	BATT Connector	Charger	VCCIN Controller	PD Controller	MIPI60	USB/I2C MUX	BurnSide Bridge	Accel	TI Amp.
PCH_SML0CLK PCH_SML0DATA	PCH								Reserve		
PCH_SML1CLK PCH_SML1DATA	PCH					V			V		
SMBCLK SMBDATA	PCH						V				
EC_SMB03_CLK EC_SMB03_DAT	MECS106	V									
EC_SMB04_CLK EC_SMB04_DAT	MECS106					V		V			
EC_SMB05_CLK EC_SMB05_DAT	MECS106				Reserve						
EC_SMB10_CLK EC_SMB10_DAT	MECS106		V	V							
EC_SMB00_CLK EC_SMB00_DAT	MECS106									V	
EC_SMB01_CLK EC_SMB01_DAT	MECS106										V

Check

PCIE/USB3.1

Flexible I/O	Interface	DESTINATION
0	PCI-E#1 / USB 3.1#1	None
1	PCI-E#2 / USB 3.1#2	USB DCI Debug
2	PCI-E#3 / USB 3.1#3	WLAN PCIe Gen2
3	PCI-E#4 / USB 3.1#4	None
4	PCI-E#5 / USB 3.1#5	None
5	PCI-E#6 / USB 3.1#6	None
6	PCI-E#7	None
7	PCI-E#8	None
8	PCI-E#9	M.2 SSD
9	PCI-E#10	
10	PCI-E#11 / SATA#0	
11	PCI-E#12 / SATA#1a	
12	PCI-E#13	None
13	PCI-E#14	None
14	PCI-E#15 / SATA#1b	None
15	PCI-E#16 / SATA#2	Card Reader PCIE GEN2

USB 2.0

USB 2.0 PORT#	DESTINATION
1	USB DCI Debug
2	None
3	None
4	Type-C_R
5	FPR
6	None
7	None
8	Type-C_L
9	CAM
10	BT

CLK

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	WLAN
	CLKOUT_PCIE1	M.2 SSD
	CLKOUT_PCIE2	None
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	None
	FLEX CLOCKS	DESTINATION
	ESPI_CLK	EC eSPI

Thunderbolt


	TBT PORT#	DESTINATION
TBT	0	USB Type-C_L
	1	None
	2	USB Type-C_R
	3	None


Displayport

	DDI PORT#	DESTINATION
DDI	A	4 Lane eDP
	B	None

Symbol Note :

@ : means de-pop

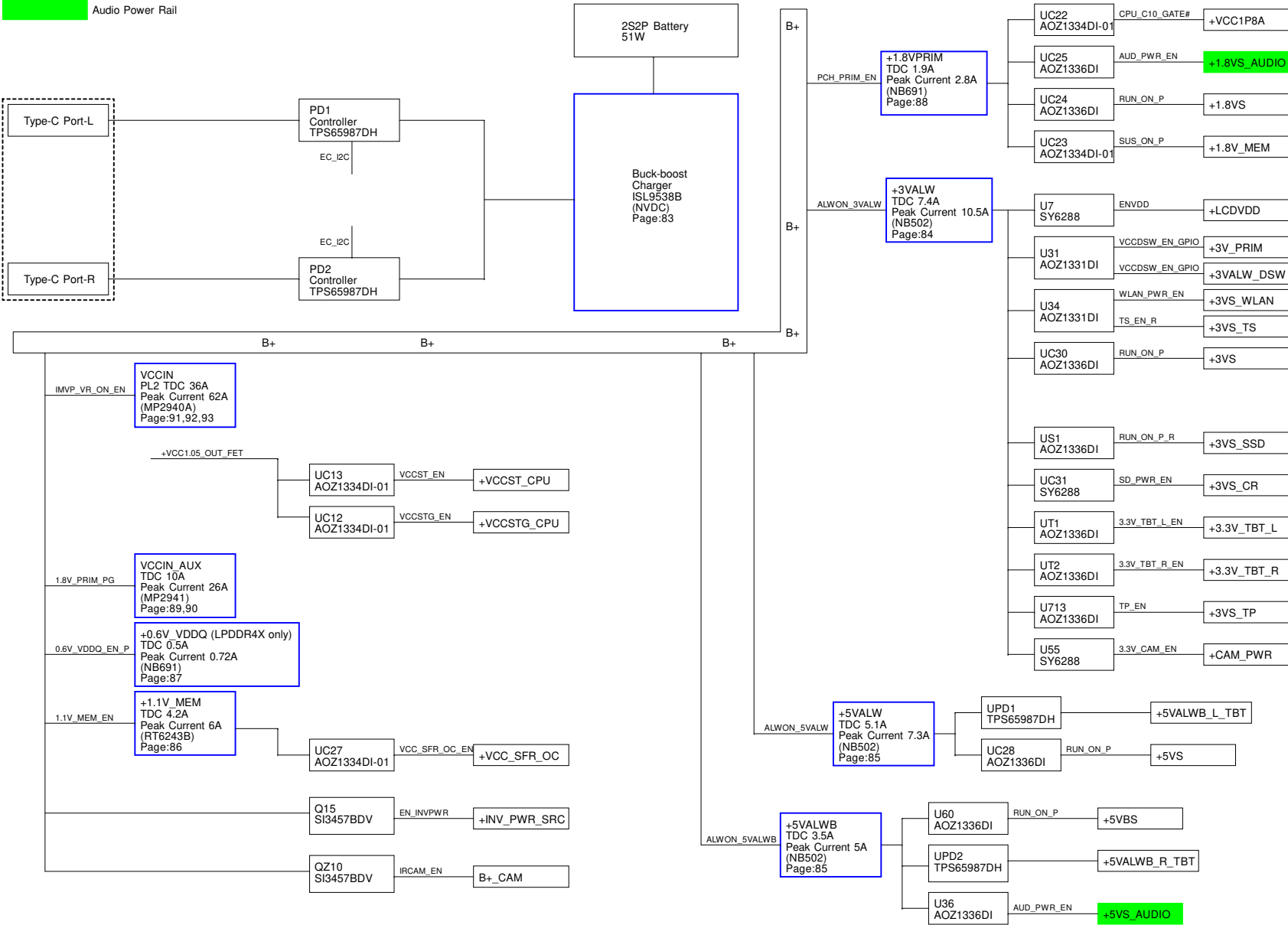
 : means Digital Ground

 : means Analog Ground

Modena POWER BLOCK DIAGRAM

Power Rail

Audio Power Rail



Power On Sequence

[AC in]

[Battery only, AC absent]

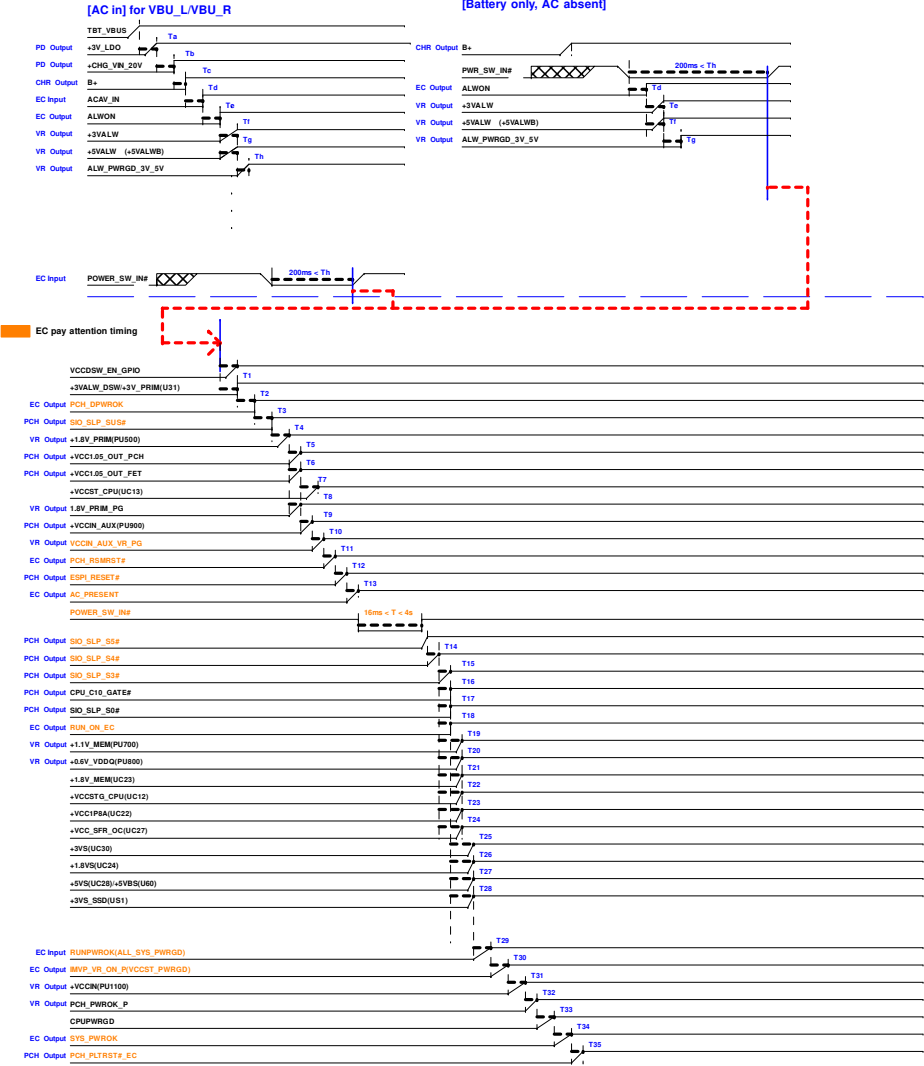
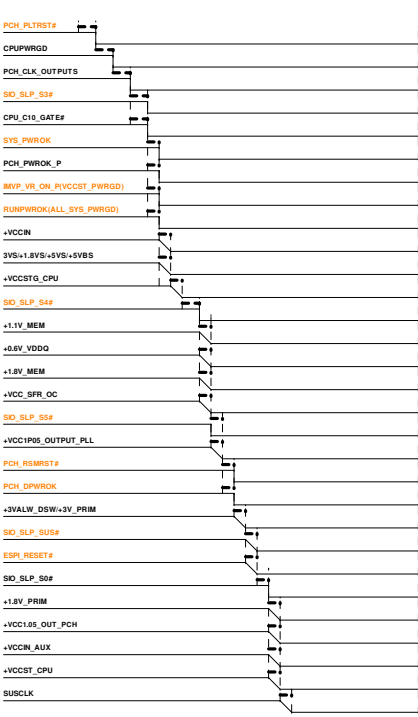
ITEM	Measure Point	Time
Ta	TBT_VBUS	To -3V_LDO
Tb	-3V_LDO	To -CHG_VIN_20V
Tc	-CHG_VIN_20V	To B+
Td	B+	To ACAP_IN
Te	ACAP_IN	To ALWON
Tf	ALWON	To -3VALW (-3VALWB)
Tg	ALWON	To ALW_PWRGD_3V_5V
Th	-3VALW	To

ITEM	Measure Point	Time
Tc	B+	To POWER_SW_IN#
Td	POWER_SW_IN#	To Low pulse width
Te	POWER_SW_IN#	To ALWON
Tf	ALWON	To -3VALW
Tg	ALWON	To -3VALW (-3VALWB)
Th	-3VALW	To ALW_PWRGD_3V_5V

ITEM	Measure Point	Time
T1	VCCDSW_EN_GPI0	To -3VALW_DSW+3V_PRIM
T2	-3VALW_DSW+3V_PRIM	To PCH_DPWR0K
T3	PCH_DPWR0K	To SIO_SLP_S5#
T4	SIO_SLP_S5#	To +1.8V_PRIM
T5	+1.8V_PRIM	To +VCC1.05_OUT_PCH
T6	+1.8V_PRIM	To +VCC1.05_OUT_FET
T7	+VCC1.05_OUT_FET	To +VCCST_CPU
T8	+1.8V_PRIM	To +1.8V_PRIM_PG
T9	+1.8V_PRIM_PG	To +VCCIN_AUX
T10	+VCCIN_AUX	To +VCCIN_AUX_VR_PG
T11	+VCCIN_AUX_VR_PG	To PCH_RSMRST#
T12	PCH_RSMRST#	To ESP_RESET#
T13	ESP_RESET#	To AC_PRESENT
T14	SIO_SLP_S5#	To SIO_SLP_S4#
T15	SIO_SLP_S4#	To SIO_SLP_S3#
T16	SIO_SLP_S3#	To CPU_C10_GATE#
T17	SIO_SLP_S4#	To SIO_SLP_S5#
T18	SIO_SLP_S4#	To RUN_ON_EC
T19	SIO_SLP_S4#	To +1.1V_MEM
T20	SIO_SLP_S4#	To +0.6V_VDDQ
T21	SIO_SLP_S4#	To +1.8V_MEM
T22	SIO_SLP_S4#	To +1.8V_MEM
T23	SIO_SLP_S4#	To +VCC1P0A
T24	SIO_SLP_S4#	To +VCC_SFR_OC
T25	RUN_ON_EC	To +3VS
T26	RUN_ON_EC	To +1.8VS
T27	RUN_ON_EC	To +3VS+3VBS
T28	RUN_ON_EC	To +3VSX3_S50
T29	RUN_ON_EC	To +SSD_PWR#
T30	RUN_ON_EC	To +SSD_PWR#
T31	+3VS	To RUNPWR0K
T32	RUNPWR0K	To BVP_VR_ON_PVCCST_PWRGD
T33	BVP_VR_ON_P	To +VCCIN
T34	+VCCIN	To PCH_PWR0K_P
T35	PCH_PWR0K_P	To CPU_PWRGD
T36	CPU_PWRGD	To SYS_PWR0K
T37	SYS_PWR0K	To PCH_PLTRST#_EC

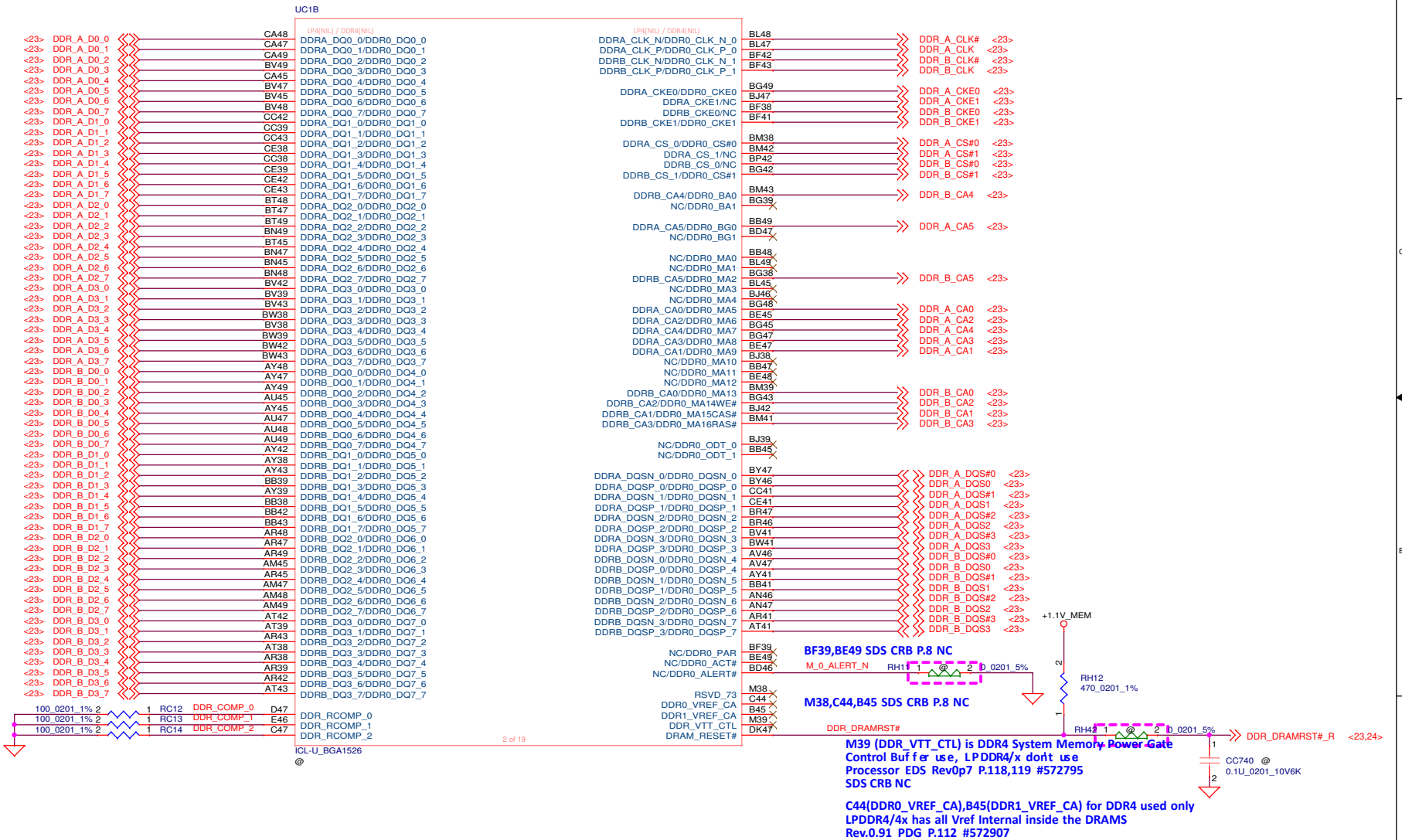
Power Down Sequence

EC pay attention timing





# Memory connection refer 573975 Rev1P1



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# Memory connection refer 573975 Rev1P1

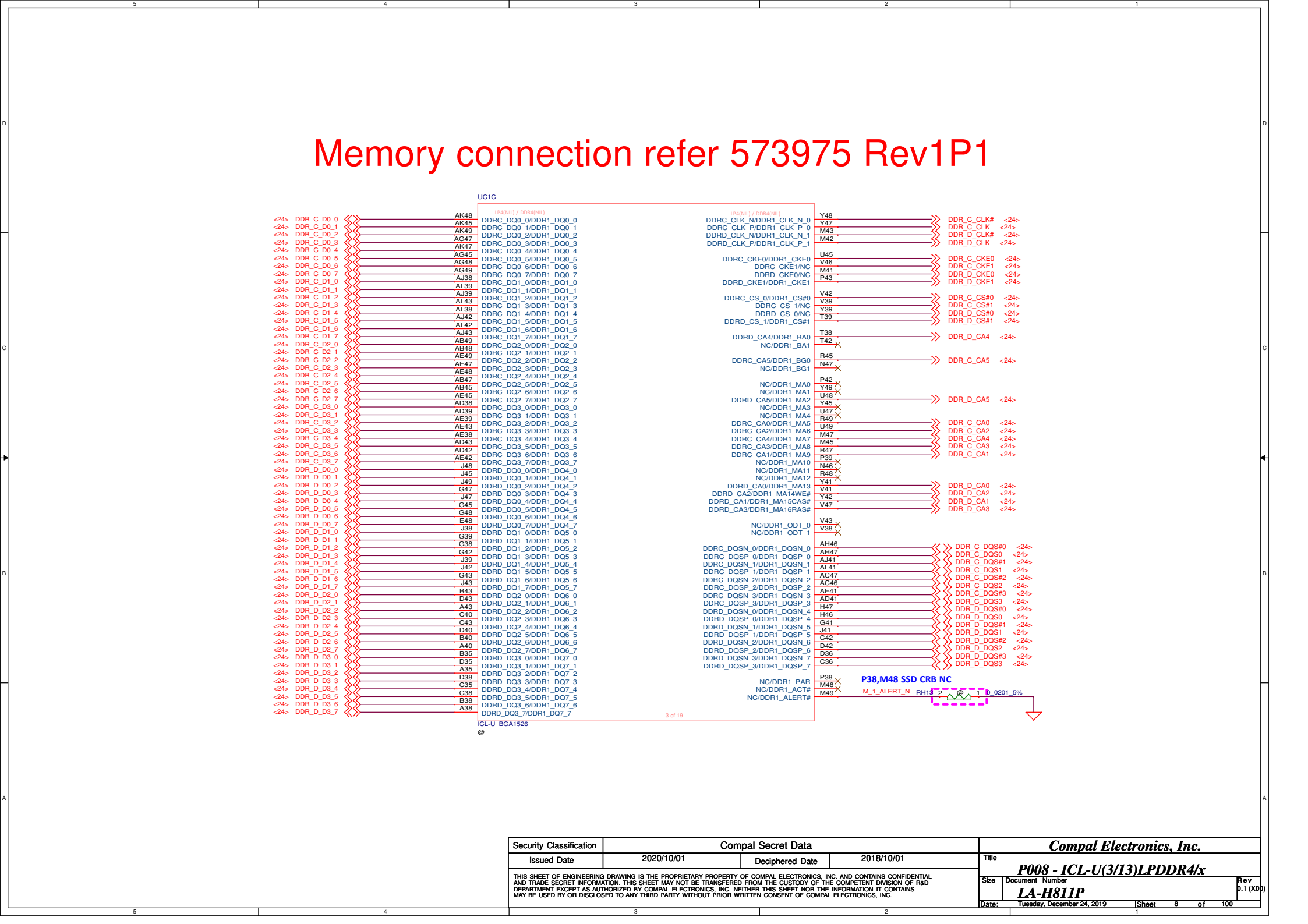
UC1C

3 of 19

ICL-U\_BGA1526

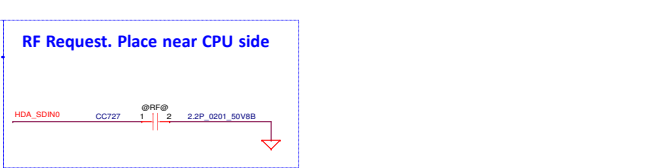
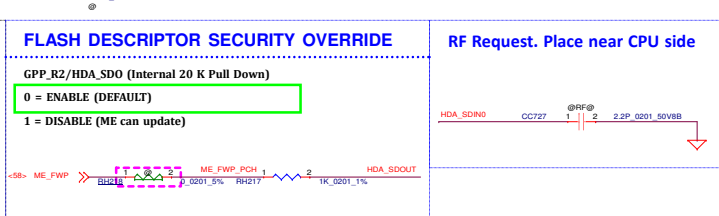
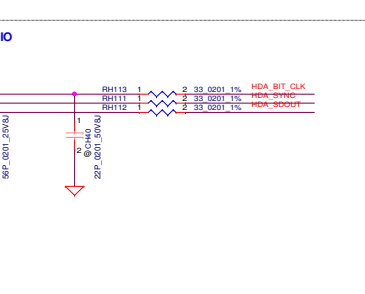
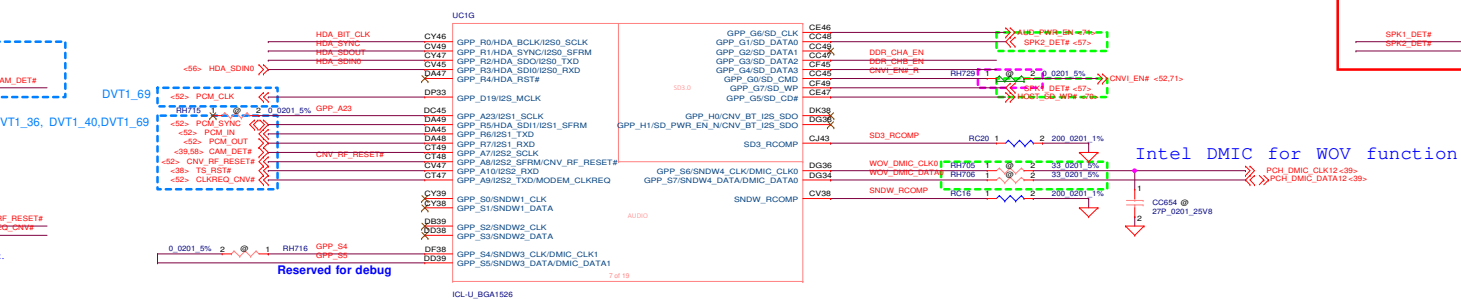
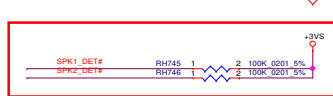
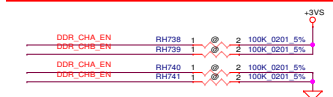
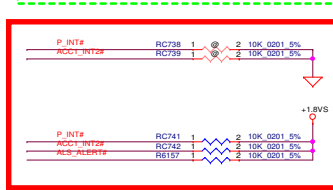
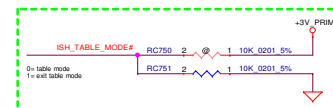
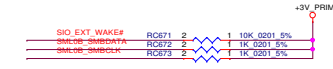
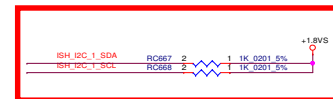
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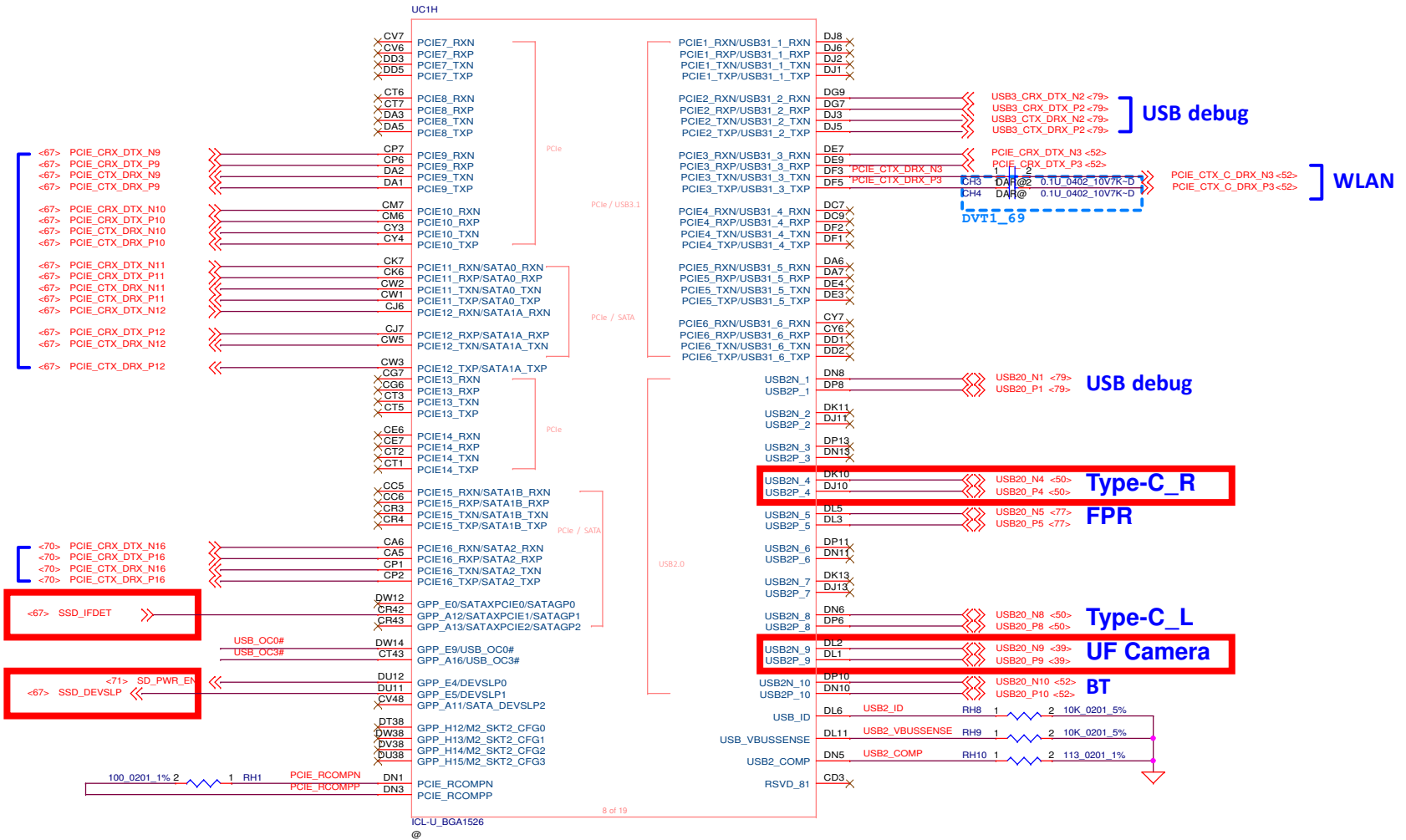
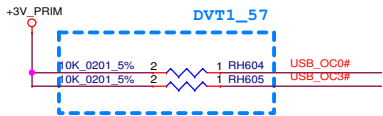


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PCIe SSDX4  
PCIe Gen3

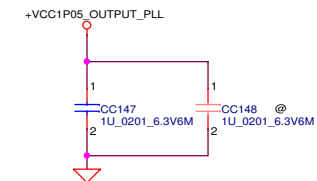
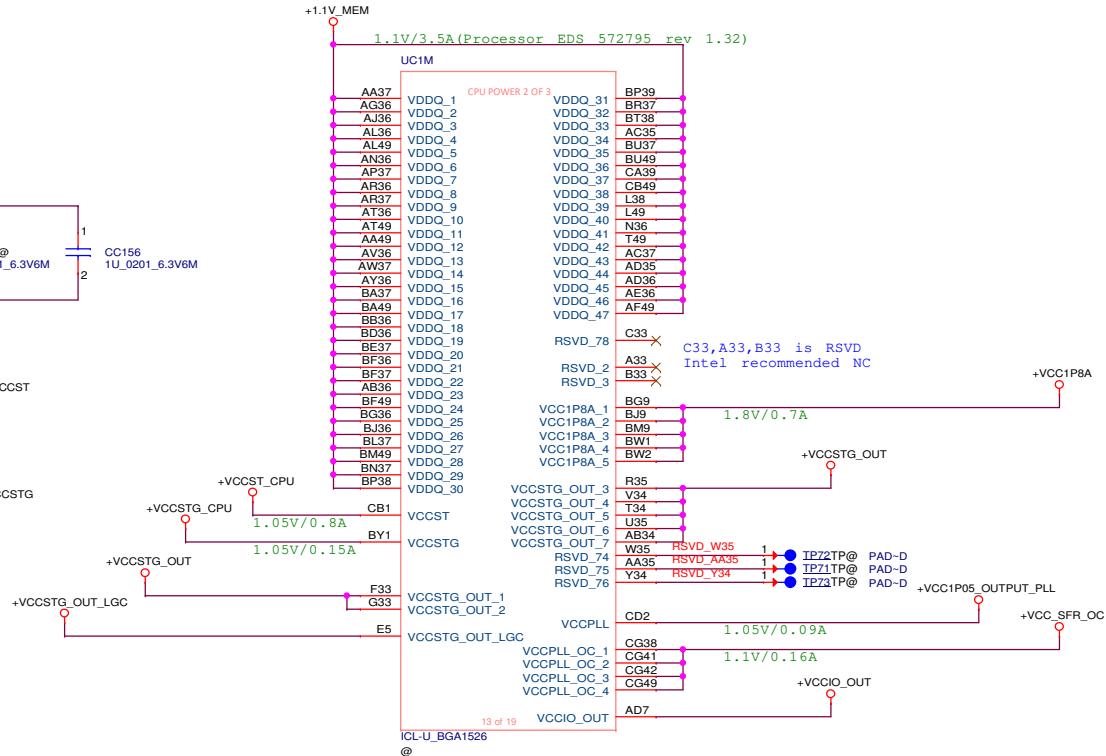
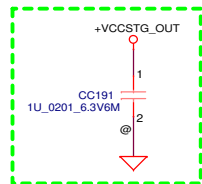
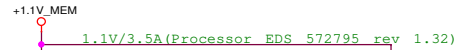
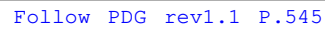
CardreaderX1  
PCIe Gen2



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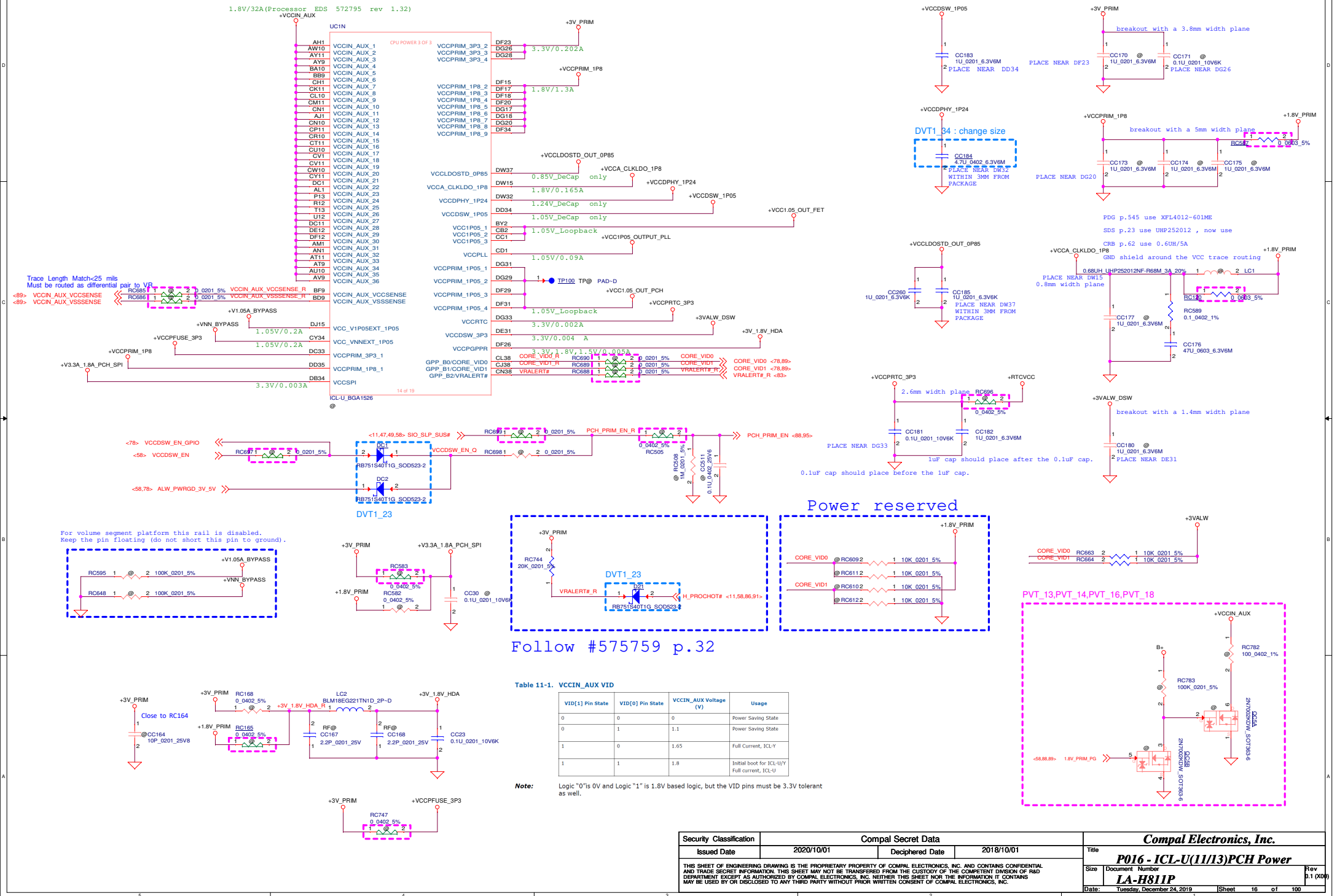




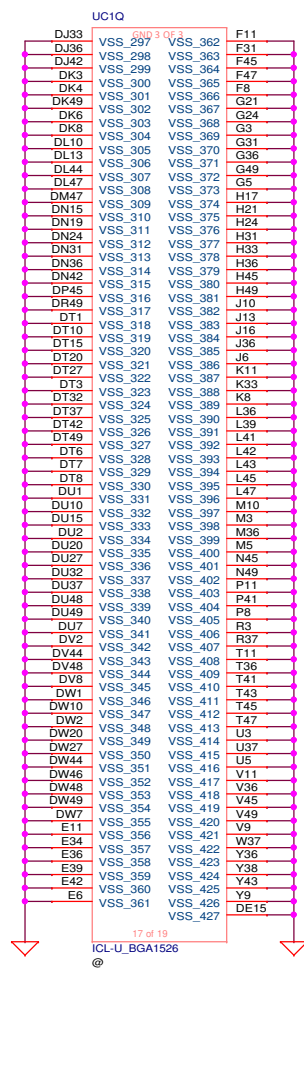
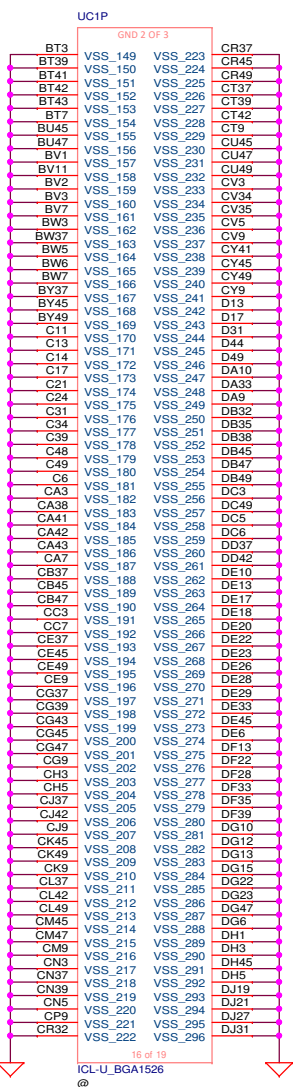
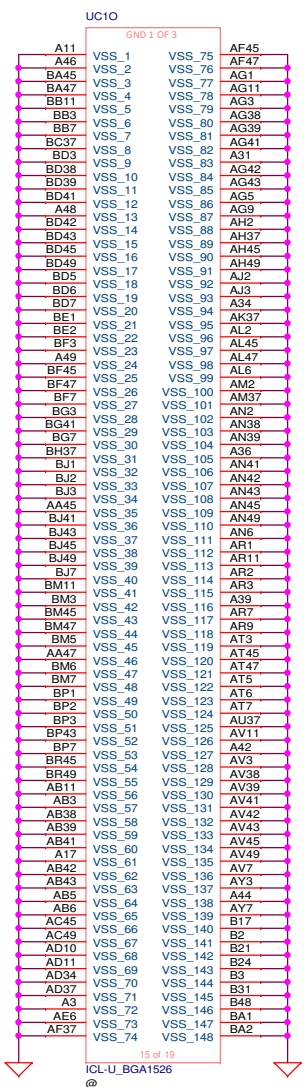


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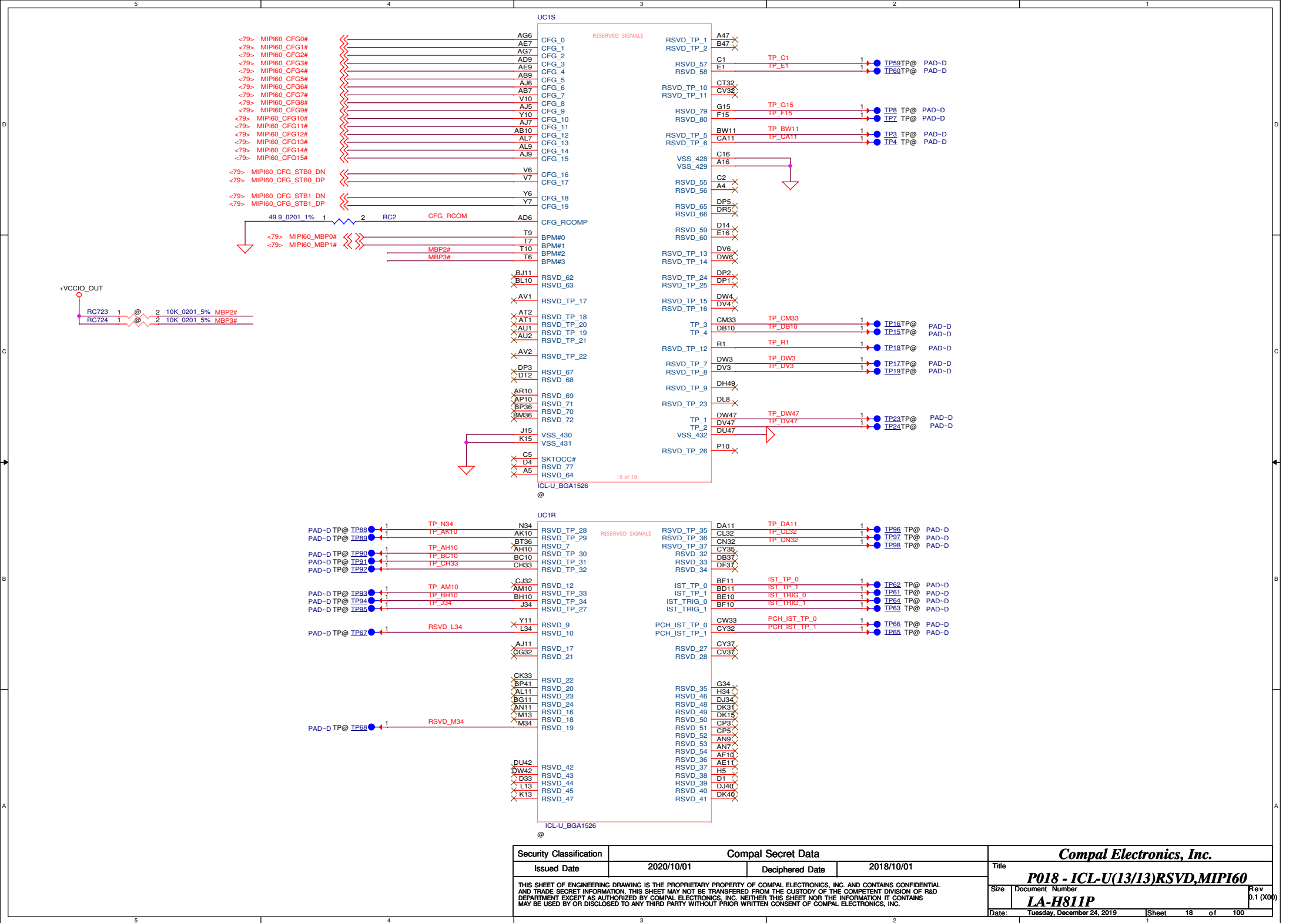


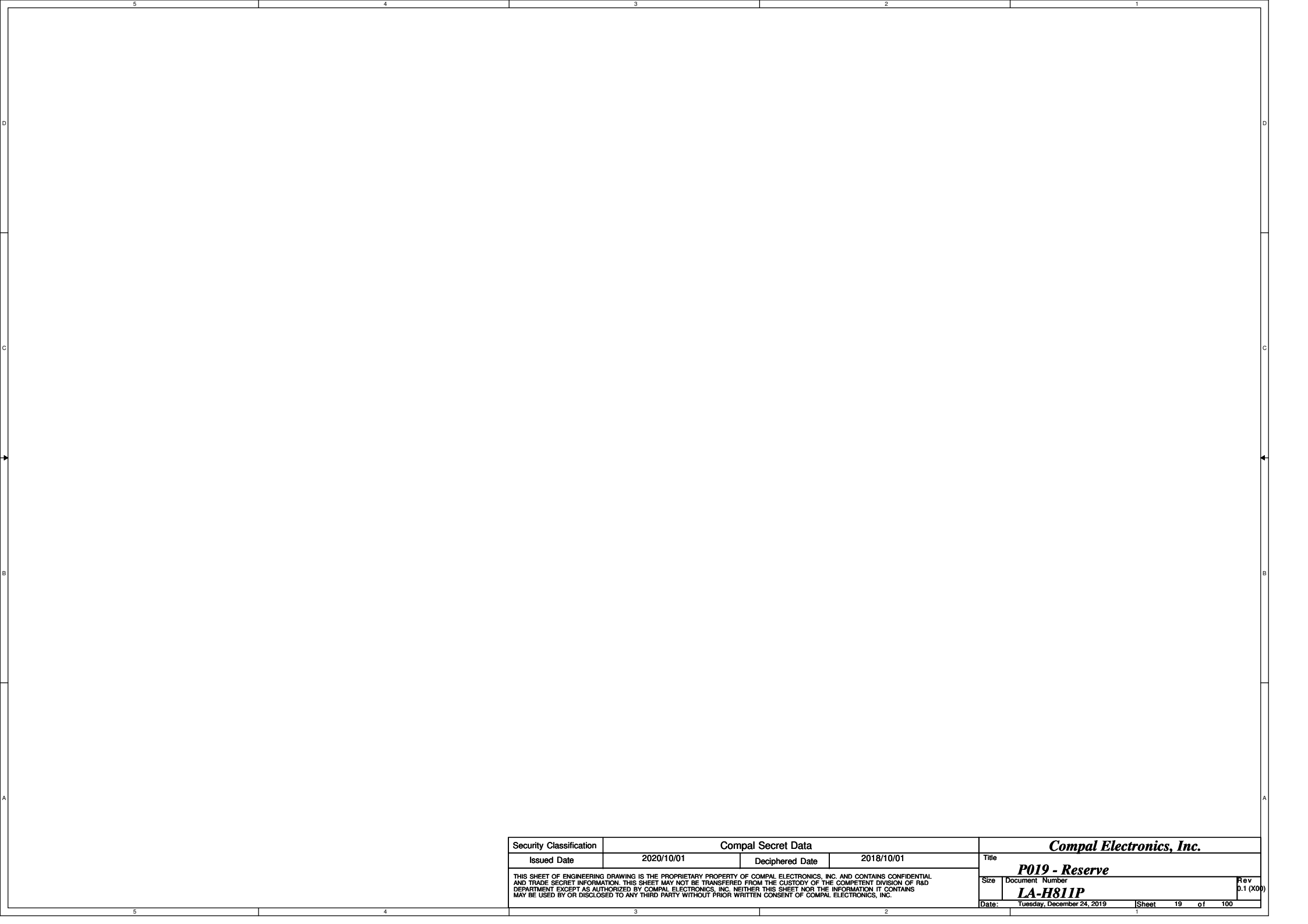




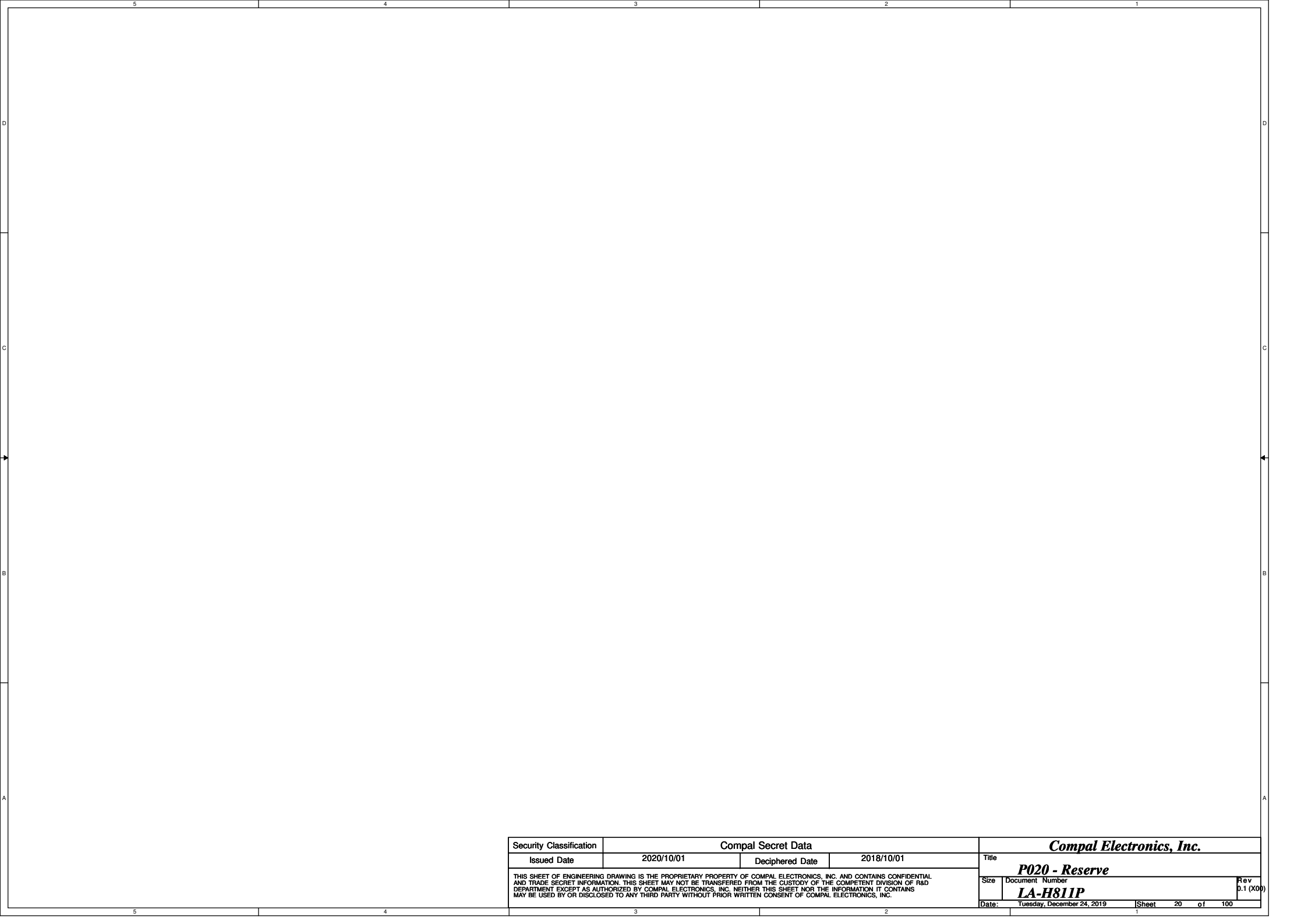


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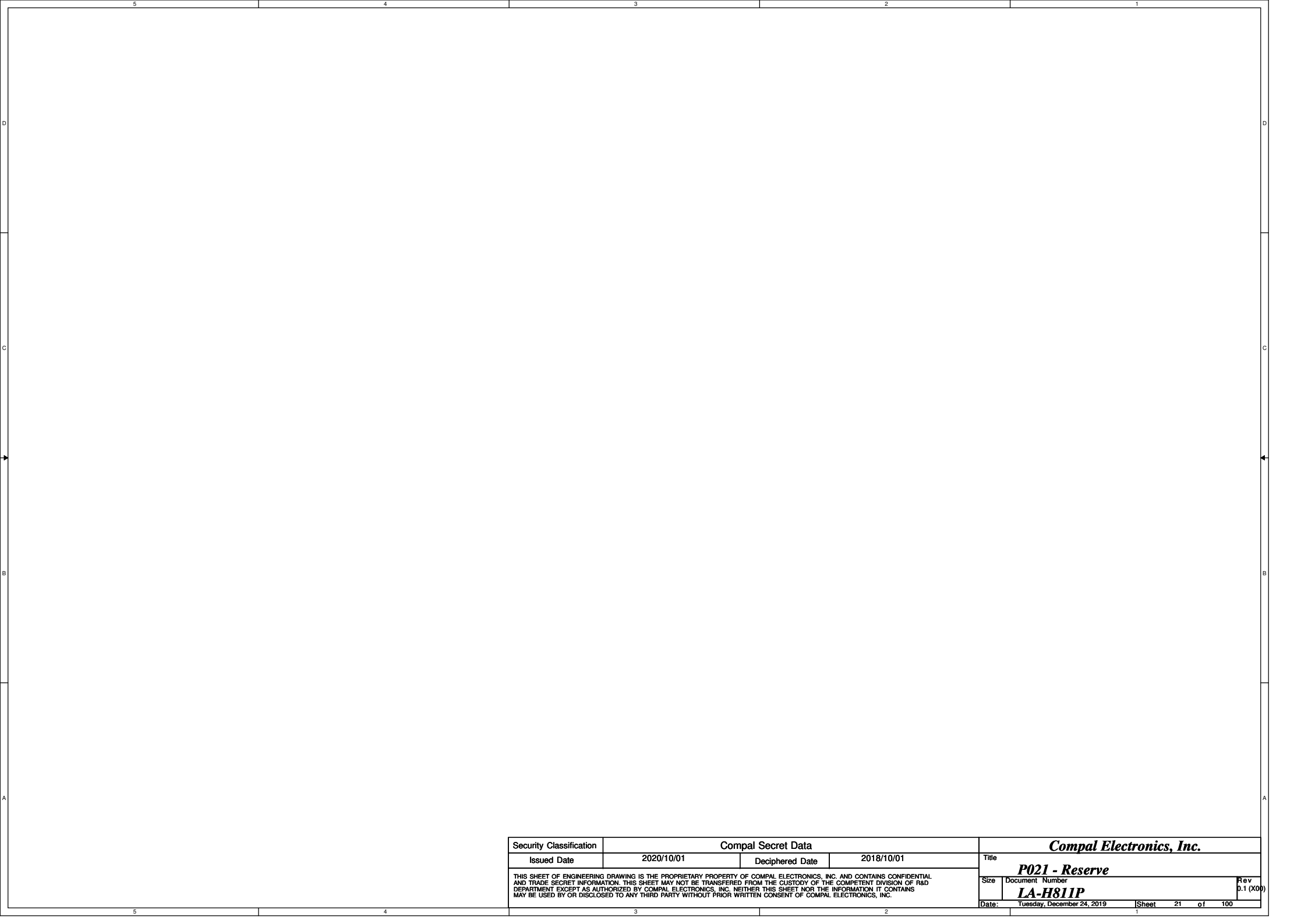




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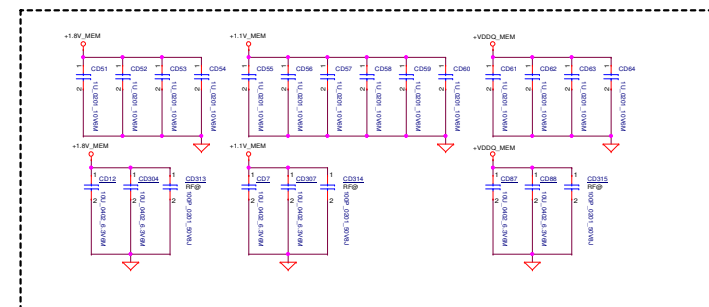
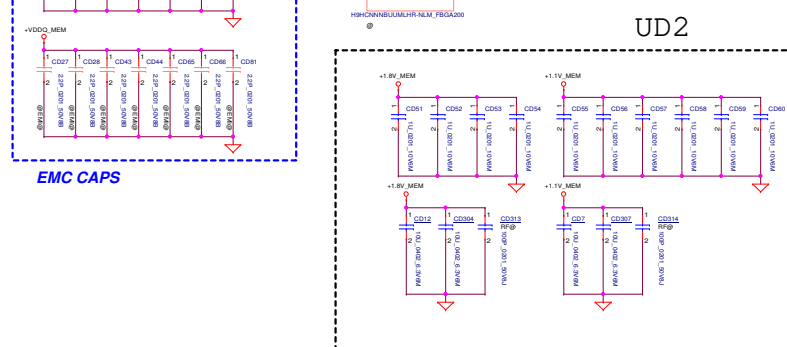
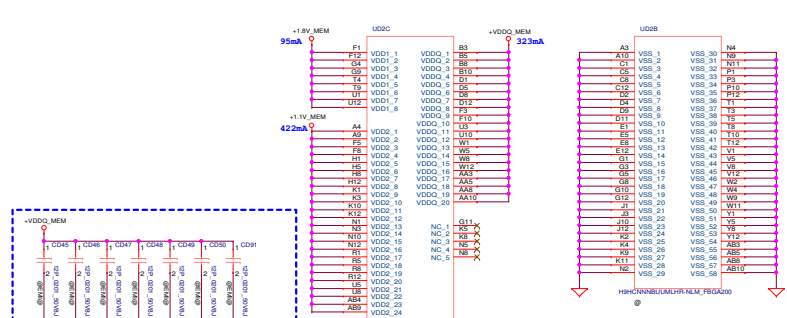


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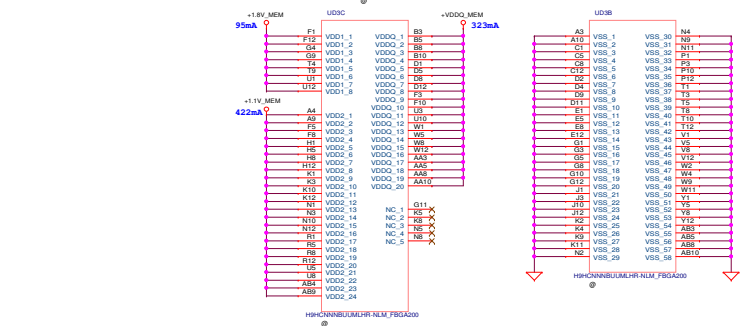
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# DDRB

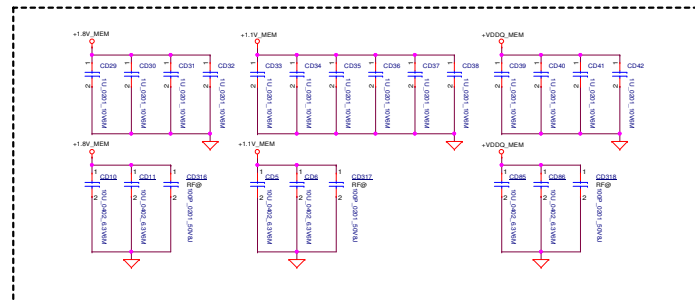


Memory connection refer 573975 Rev1P1

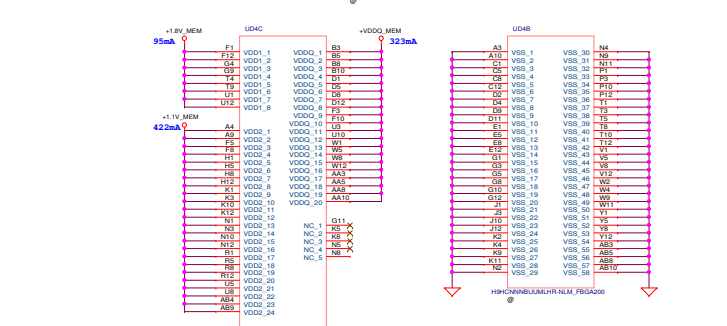
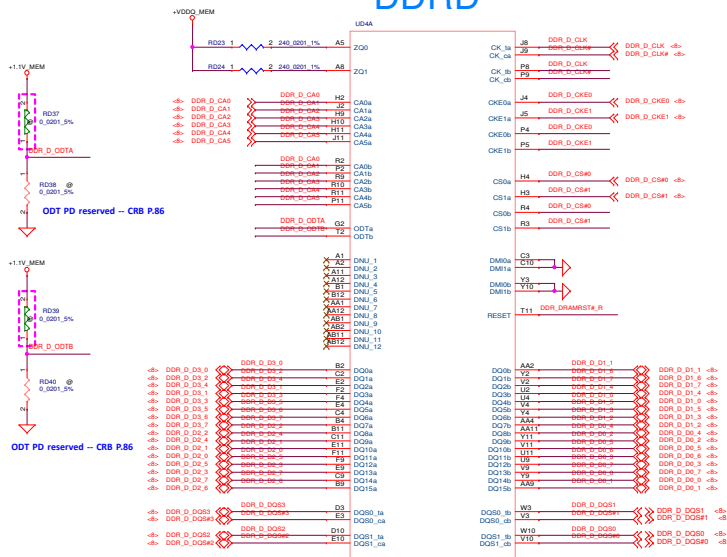
## DDRC



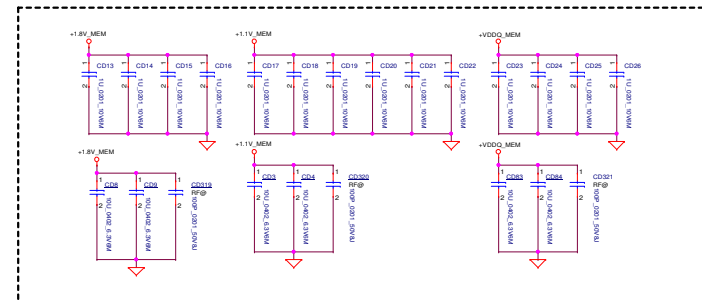
## UD3



## DDRD

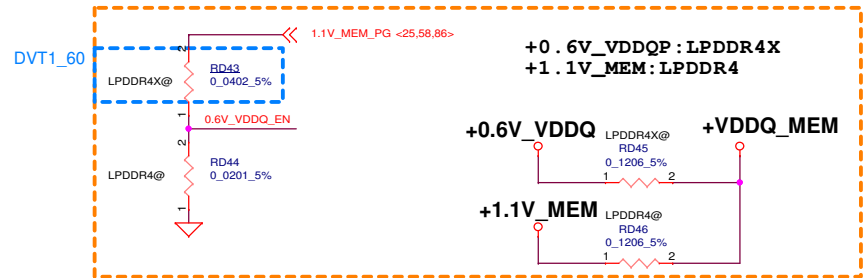
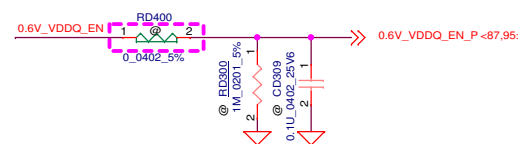
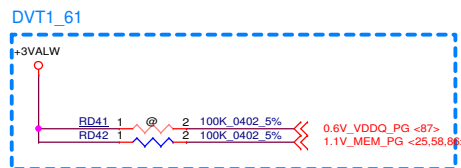


## UD4

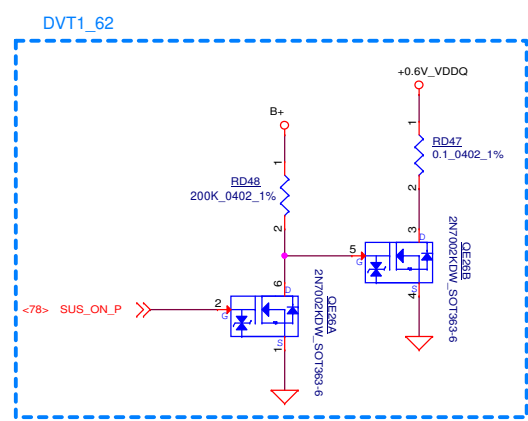


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Issued Date		Declassified Date		<b>Compul Electronics, Inc.</b> <b>D024 - LPDDR4x Channel C/D</b> <b>LA-H811P</b>	
2020/10/01		2018/10/01		S/N: [Redacted] Rev: 1 (2020) Date: Tuesday, December 24, 2019 Sheet 24 of 100	
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	RD43	RD45	RD44	RD46
LPDDR4 (1.1V) :	@	@		
LPDDR4X (1.1V&0.6V) :			@	@





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				Size	Document Number
				LA-H811P	
Date: Tuesday, December 24, 2019				Sheet	31 of 100
				Rev	0.1 (X00)



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				Size	Document Number
				LA-H811P	
Date: Tuesday, December 24, 2019				Sheet	35 of 100
				Rev	0.1 (X00)

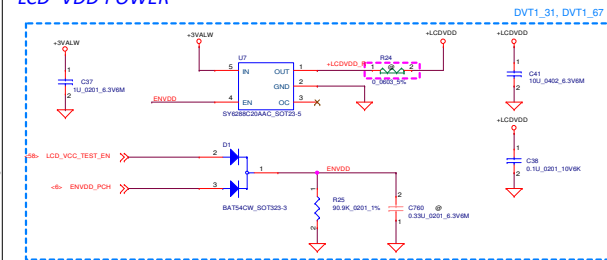


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				Size	Document Number
				LA-H811P	
				Date:	Tuesday, December 24, 2019
				Sheet	36 of 100
				Rev	0.1 (X00)

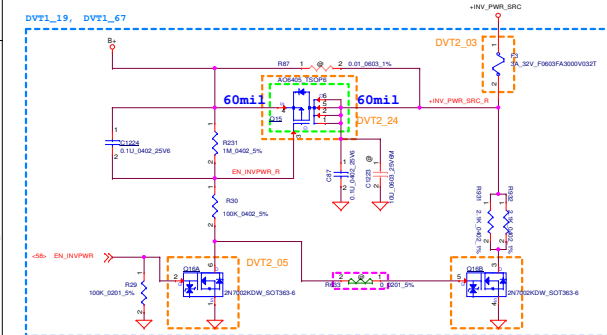


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				LA-H811P	

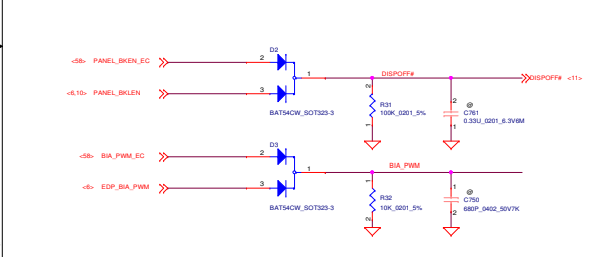
*LCD VDD POWER*



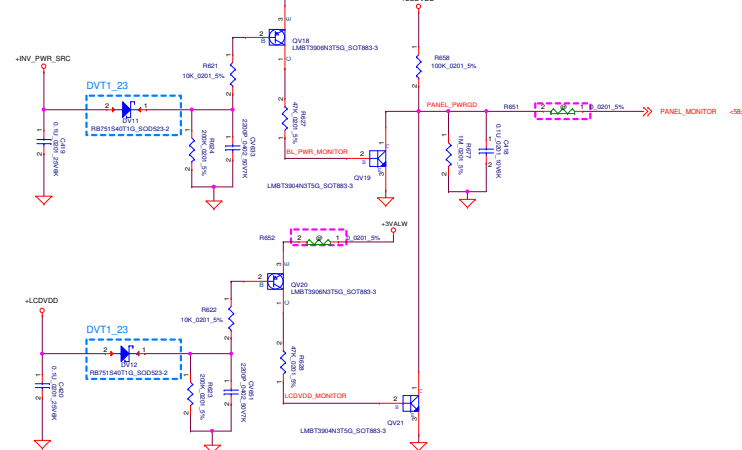
*eDP BackLight Power*



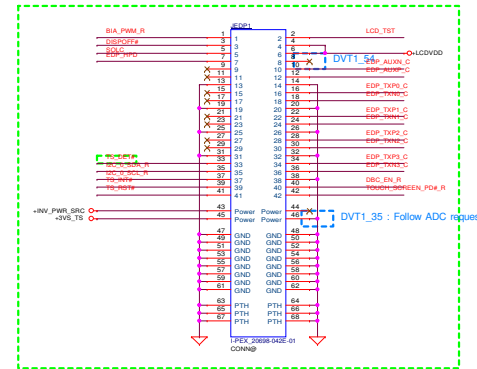
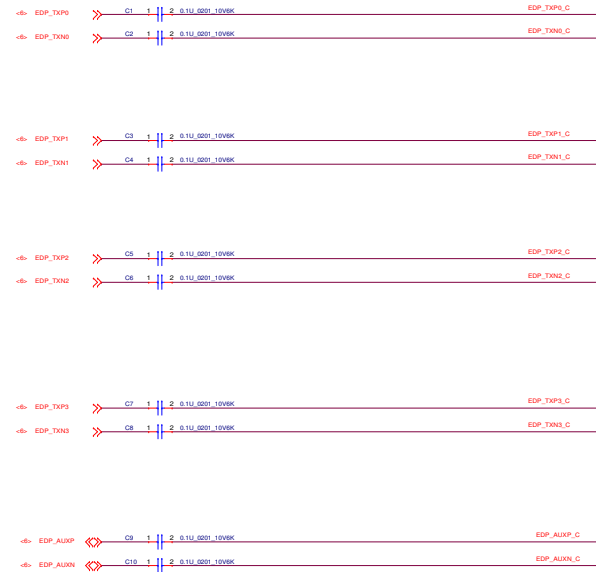
### BackLight PWM Control



For BL\_PWR\_SRC & LCDVDD monitor

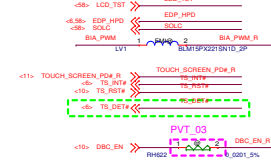


eDP Conn

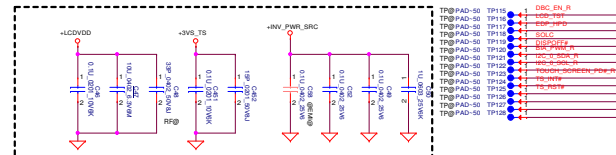


Bit Rate	Lane Supports (max # of lanes)	Peak Bandwidth
1.62 Gb/s (P8R)	4	4 x 162 Mb/s = 648 Mb/s
2.7 Gb/s (P8R)	4	4 x 270 Mb/s = 1080 Mb/s
5.4 Gb/s (P8R2)	4	4 x 540 Mb/s = 2160 Mb/s
8.1 Gb/s (P8R3)	4	4 x 810 Mb/s = 3240 Mb/s

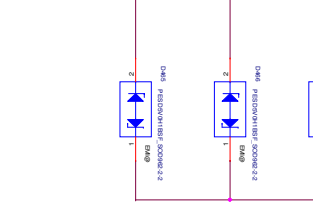
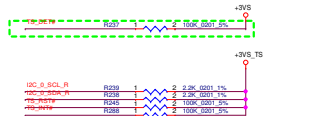
eDP\* Bit Rates 8.1 Gb/s (HBR3)  
In TCON side, RX Equalization CTLE + DFE  
DFE=Decision feedback equalizer  
CTLE=Constant time linear Equalizer



For factory test request



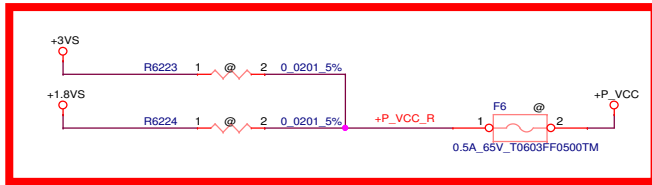
Connector	Pin	NAME	IN/OUT	FUNCTION
CNI	1	ISTOP	I	High: Normal Operation Low: Stop Scanning Build-in pull-up (to 3.3 V) resistor 250k
	2	IC BDA	I/O	IC Data Open drain output, pull-up resistor at Host head
	3	IC BCL	I/O	IC Clock Open drain output, pull-up resistor at Host head
	4	NC	-	No Connection
	5	NC	-	No Connection
	6	/IC IRQ	O	IC Data Ready Output "LOW" when data ready to send Open drain output, pull-up resistor at Host head
	7	/RESET	I	Hardware RESET Low Active Stop operation when pull "LOW" Build-in pull-up (to 3.3 V) resistor 100k
	8	VCC +3.3V	-	+ 3.3 volts TLP power input No Connection
	9	GND	-	Signal
	10	GND	-	Signal



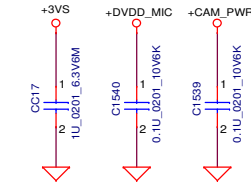
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				<b>P038 - eDP Touch Screen</b>	1 of 100
				<b>LA-H811P</b>	
				Issue Date	2019.05.20
				Drawn By	05
				Check By	01
				Rev By	01

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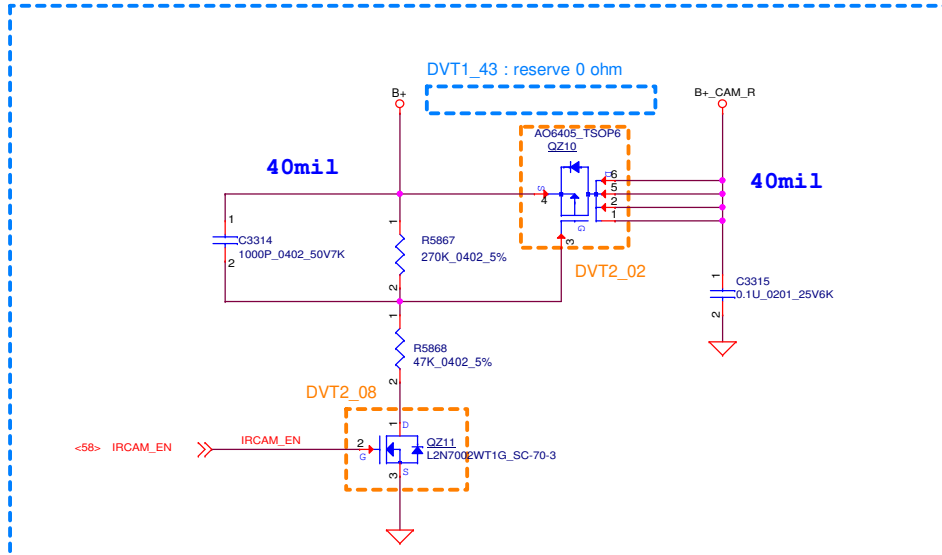
TP@PAD-50 TP134 1 ISH\_I2C\_1\_SCL\_R  
 TP@PAD-50 TP135 1 ISH\_I2C\_1\_SDA\_H  
 TP@PAD-50 TP136 1 ALS\_ALERT#\_R  
 TP@PAD-50 TP145 1 CAM\_DET#\_R



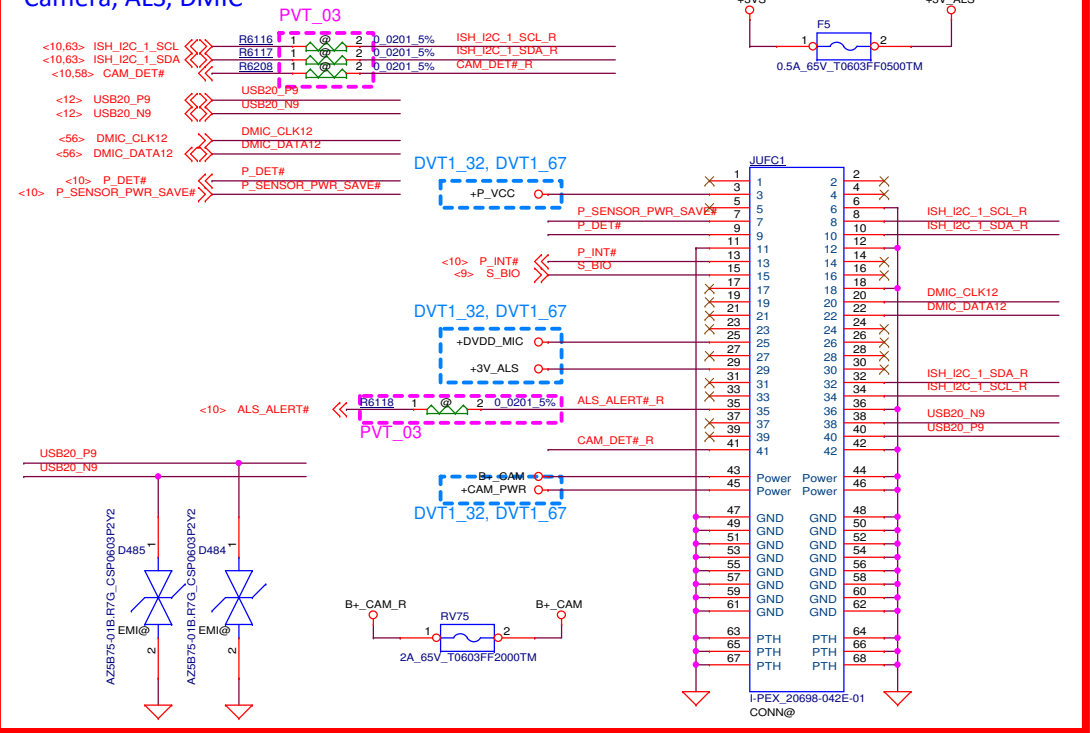
Bypass cap close to CONN



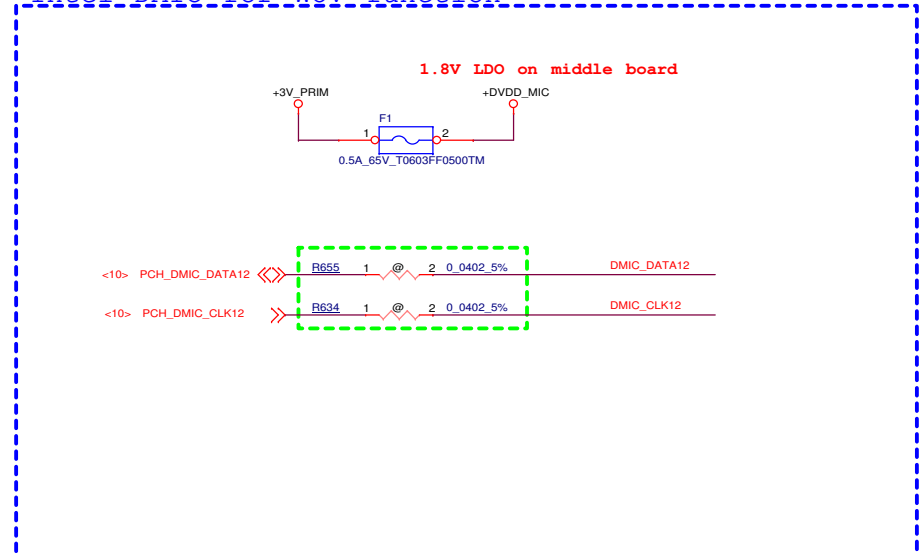
DVT1\_20, DVT1\_67



## Camera, ALS, DMIC



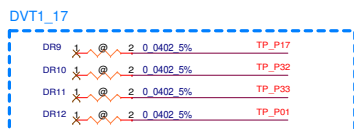
## Intel DMIC for WOV function



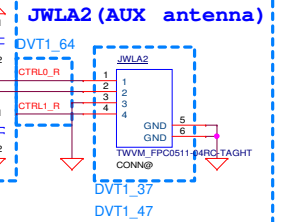
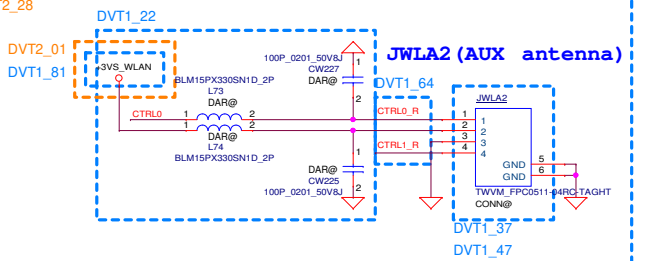
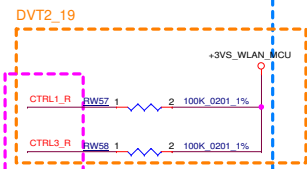
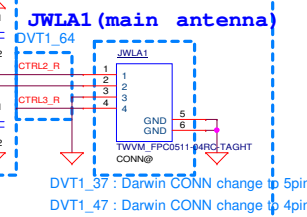
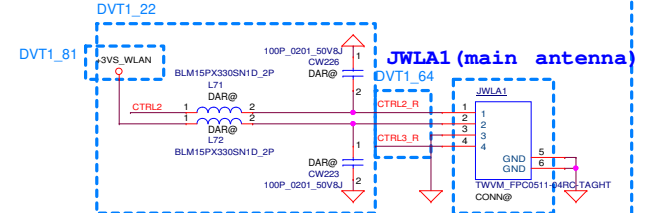
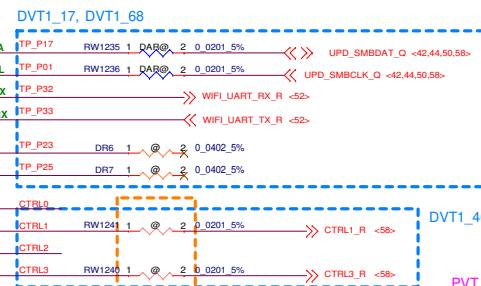
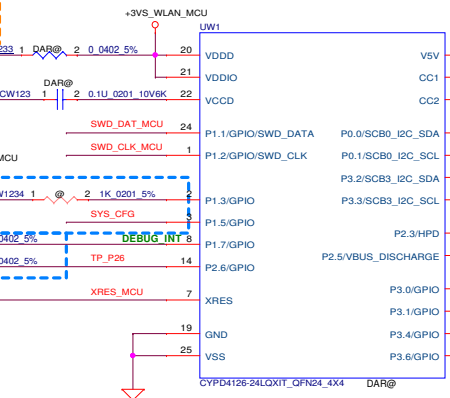
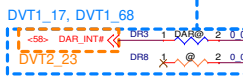
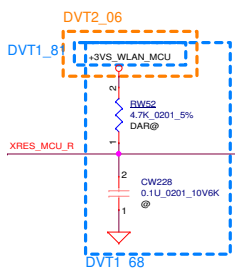
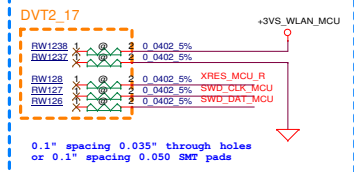
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Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P039 - UF Camera,MIC,ALS
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				LA-H811P	
				Date:	Tuesday, December 24, 2019
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# Darwin 2.0

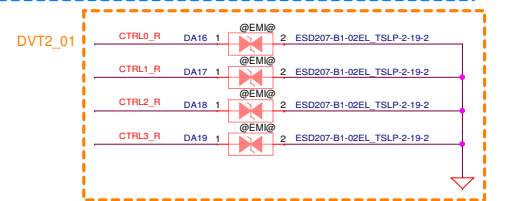
DVT1\_16 : add Darwin2.0



DVT1\_27 : reserve five test pad for FW updated



I2C ADDR	I2C Slave Address
NC	0x72 (default)
Pull up 3.3V	0x34



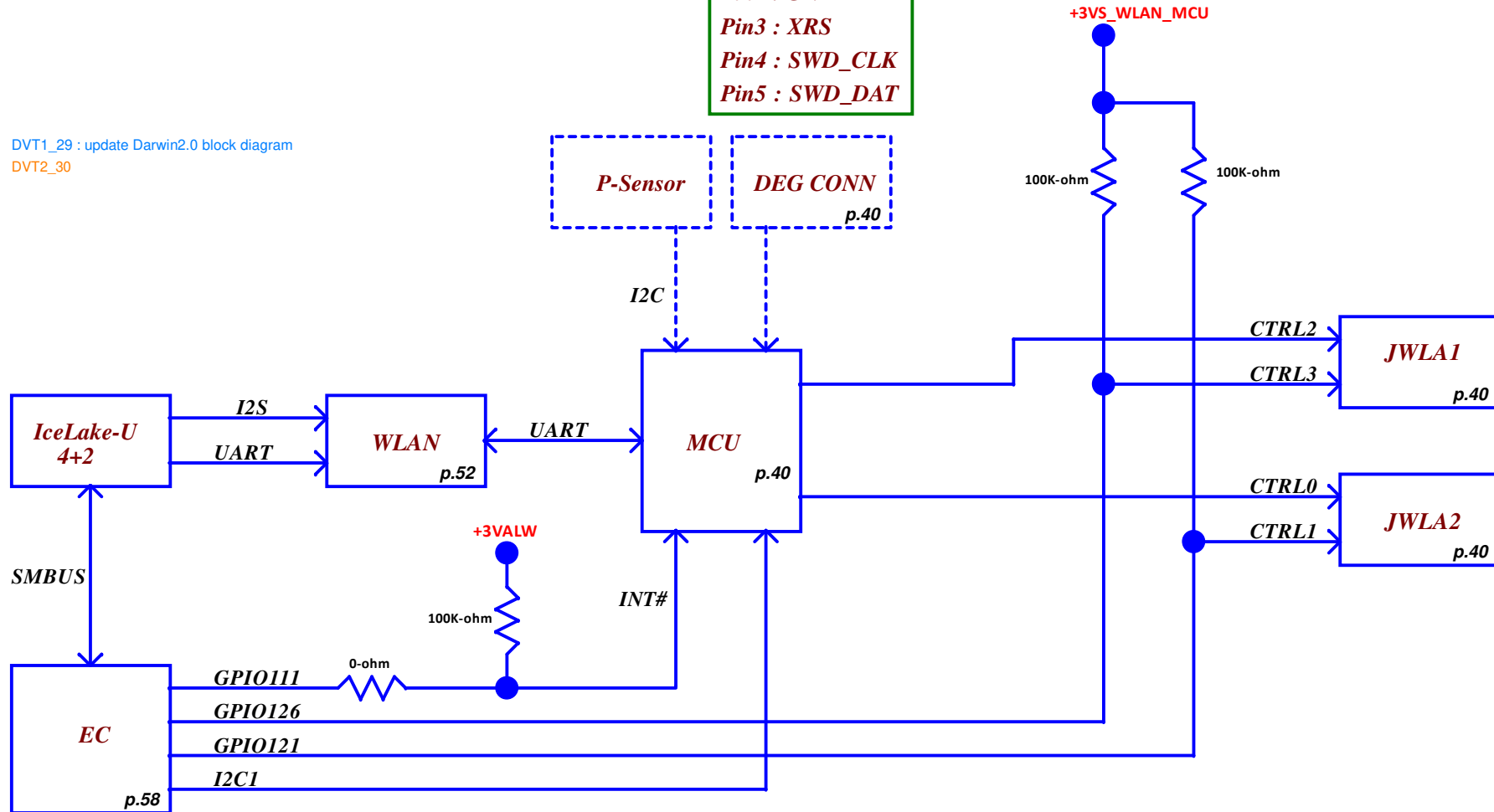
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		Size	Document Number
		LA-H31P	
		Date	Tuesday, December 24, 2019
		Sheet	40 of 100
		Rev	01 (X00)



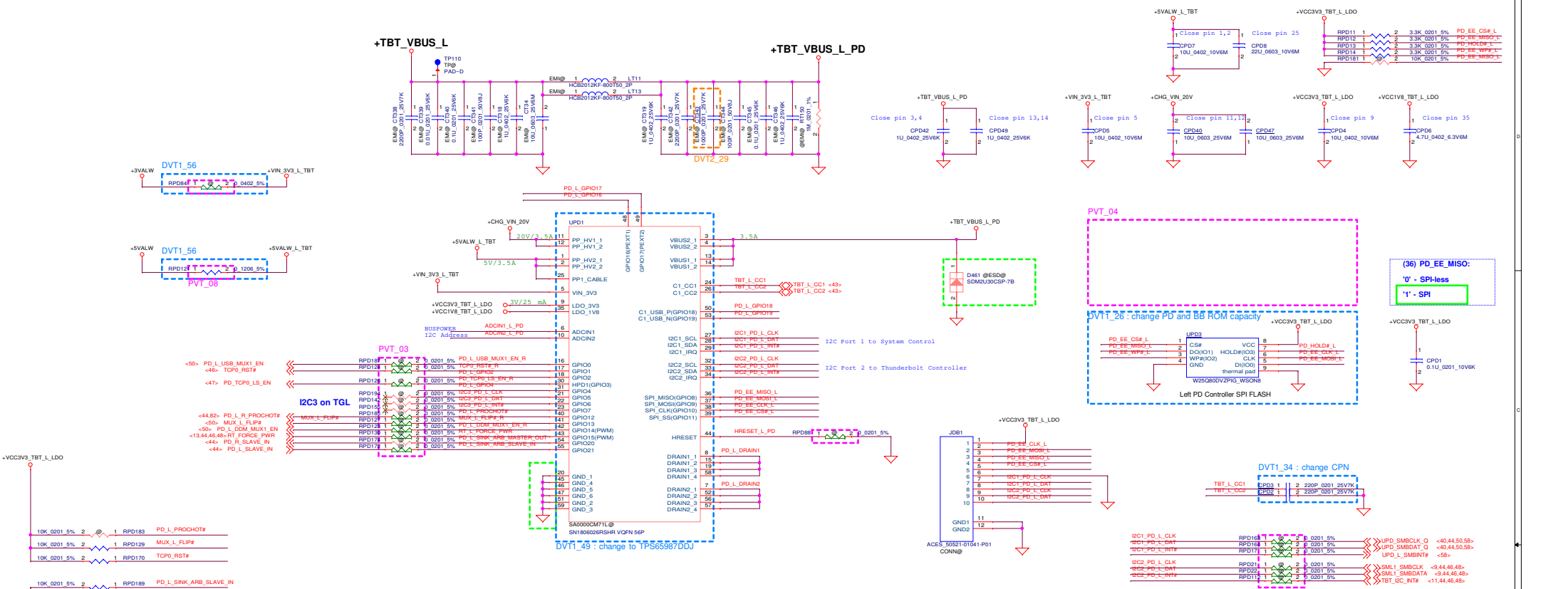
## Pin definition

*Pin1 : +3V*  
*Pin2 : GND*  
*Pin3 : XRS*  
*Pin4 : SWD\_CLK*  
*Pin5 : SWD\_DAT*

DVT1\_29 : update Darwin2.0 block diagram  
DVT2\_30



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				Rev	0.1 (X00)



### BUSPOWER Config

BP\_NoWait value 0.6~1.00

### I2C Address Divider:010b

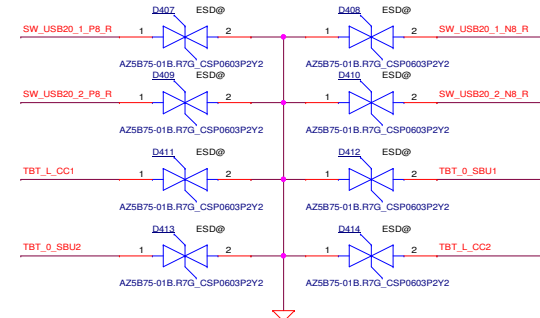
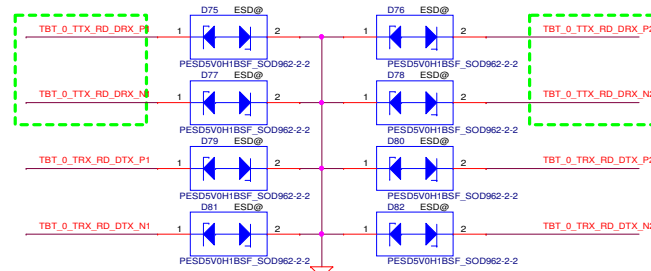
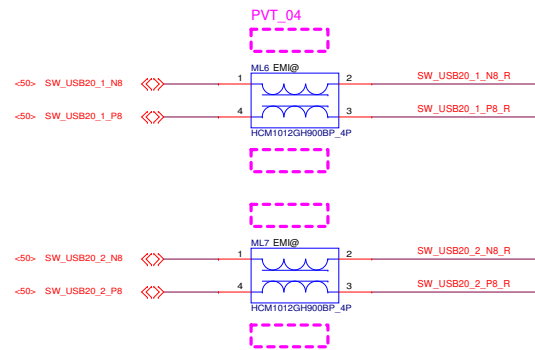
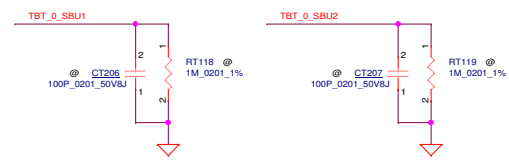
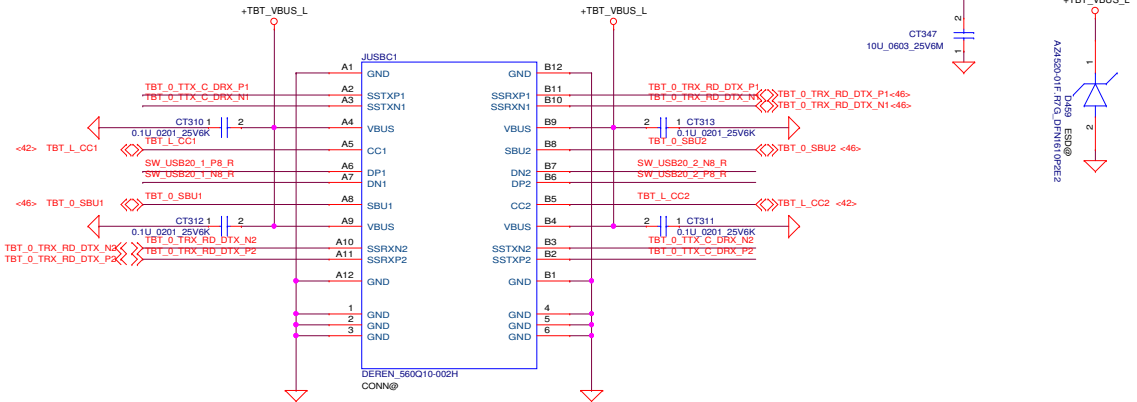
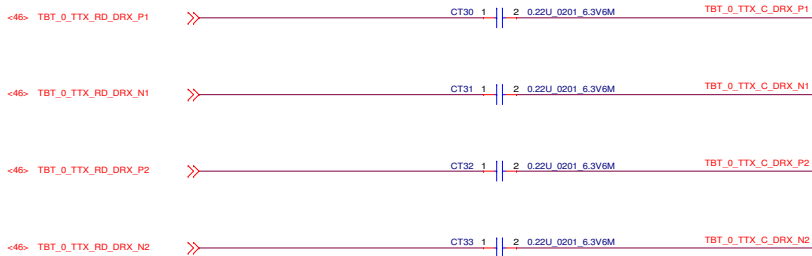
### Table 2. BUSPOWER Configuration

BP_NoWait	BP_NoWait	Configuration	Description	Recommended for
0.00	0.10	BP_NoWait	NO power switch is enabled and the device does not enter into VIL_010b	Ports that support charging or operation during a dead battery condition.
0.20	0.30	BP_NoWaitF010b	The internal pull-up resistor for the port (VIL_010b) is enabled for the port. The device does not require to be powered up or attempt to load device configuration until VIL_010b is present.	Ports that support charging or operation during a dead battery condition, and depend on on-board system components for device configuration and operation.
0.40	0.50	BP_NoWaitF010b	The internal pull-up resistor for the port (VIL_010b) is enabled for the port. The device does not require to be powered up or attempt to load device configuration until VIL_010b is present.	Ports that support charging or operation during a dead battery condition, and depend on on-board system components for device configuration and operation.
0.60	1.00	BP_NoWait	The device continues to start-up and attempt to load configuration until receiving power from VIL_010b. Once configuration is loaded, the device will remain in a low-power state until the device is loaded configuration.	Ports that support charging or operation during a dead battery condition, and do not depend on on-board system components for device configuration and operation.

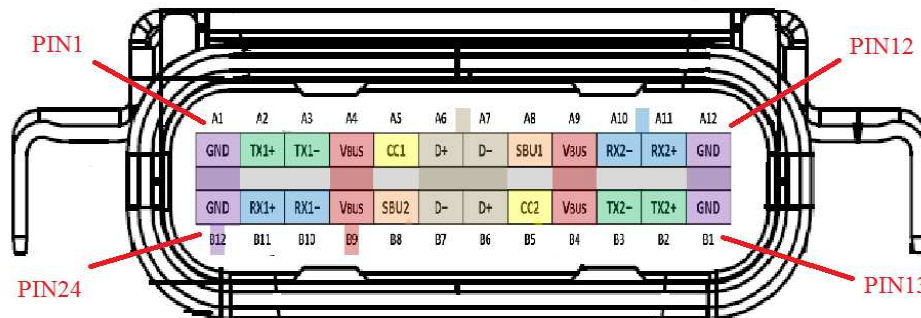
### Table 3. PC Address Selection

BP_NoWait	BP_NoWait	Configuration	PC Address Selection
0.00	0.10	BP_NoWait	0x00
0.20	0.30	BP_NoWaitF010b	0x01
0.40	0.50	BP_NoWaitF010b	0x02
0.60	1.00	BP_NoWait	0x03

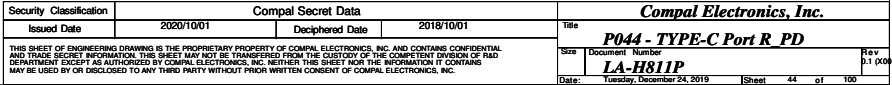
# LEFT Type-C Connector



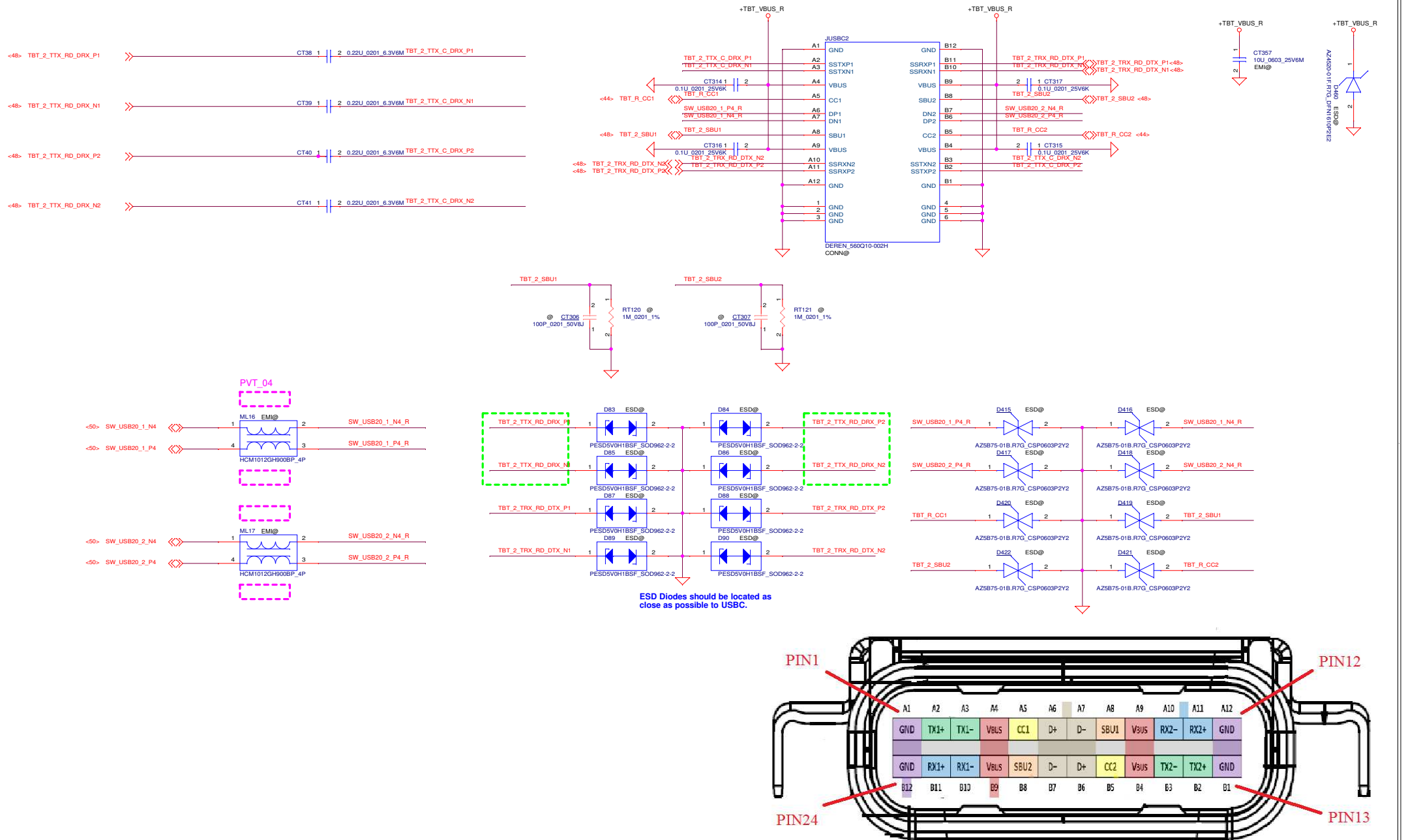
ESD Diodes should be located as close as possible to USBC.



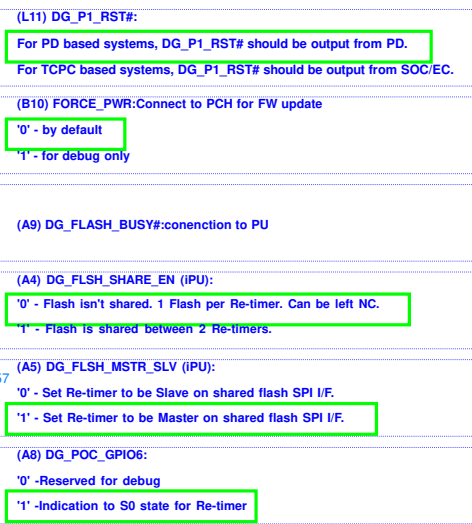
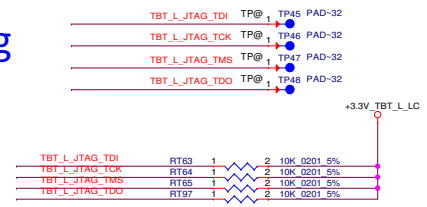
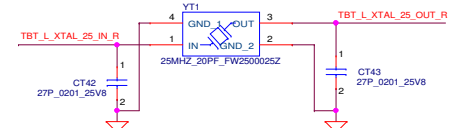
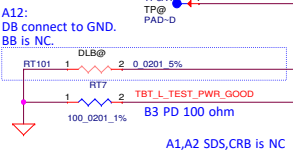
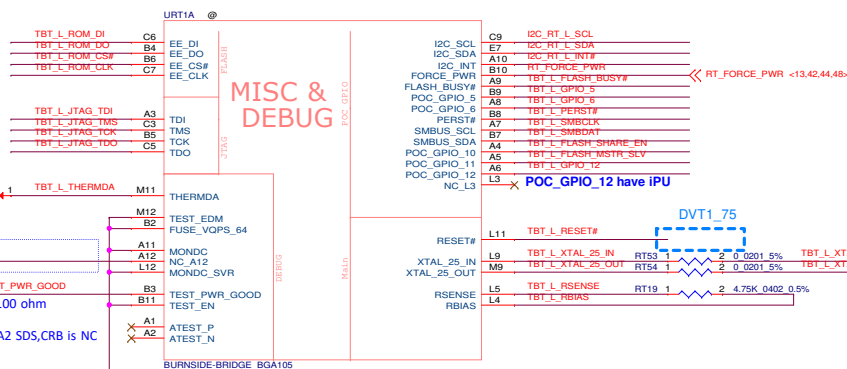
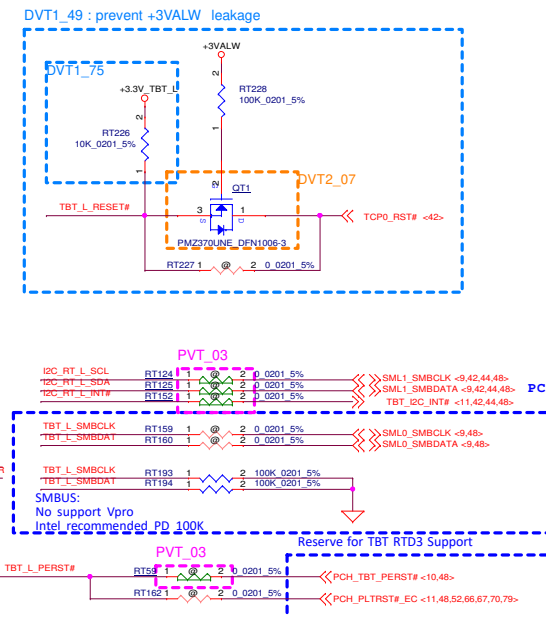
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## RIGHT Type-C Connector



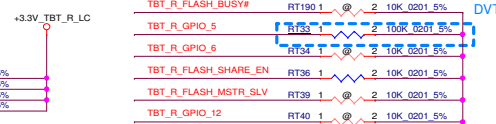
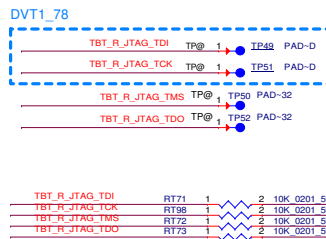
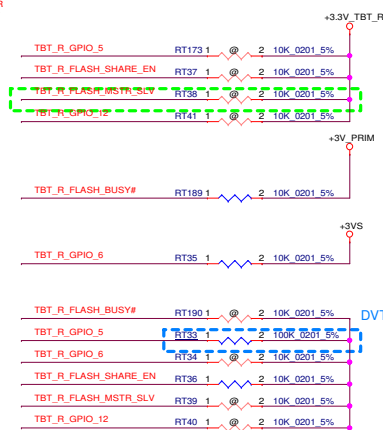
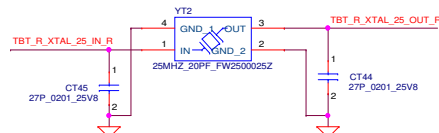
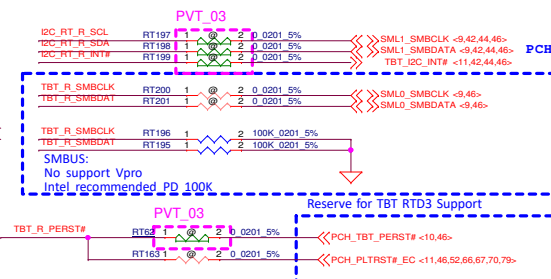
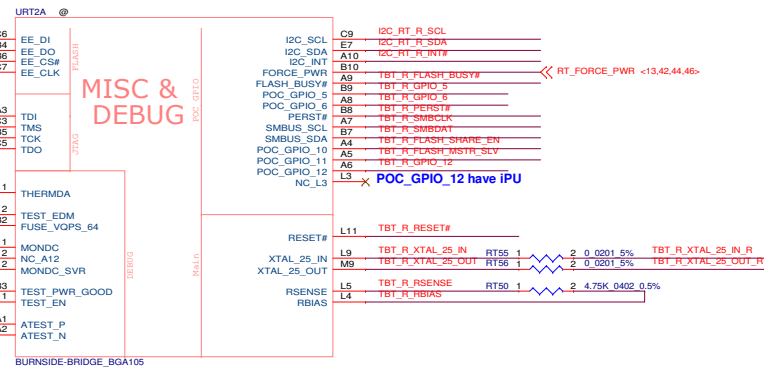
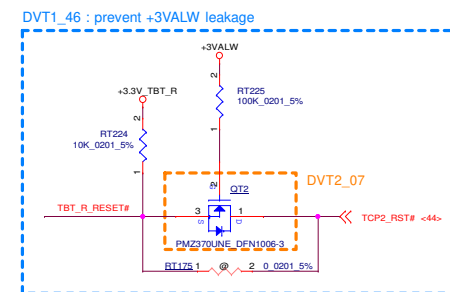
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				Size	Document Number	Rev
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(L11) DG\_P1\_RST#:   
For PD based systems, DG\_P1\_RST# should be output from PD.   
For TPCP based systems, DG\_P1\_RST# should be output from SOC/EC.

(B10) FORCE\_PWR:Connect to PCH for FW update   
'0' - by default   
'1' - for debug only

(A9) DG\_FLASH\_BUSY#:connection to PU

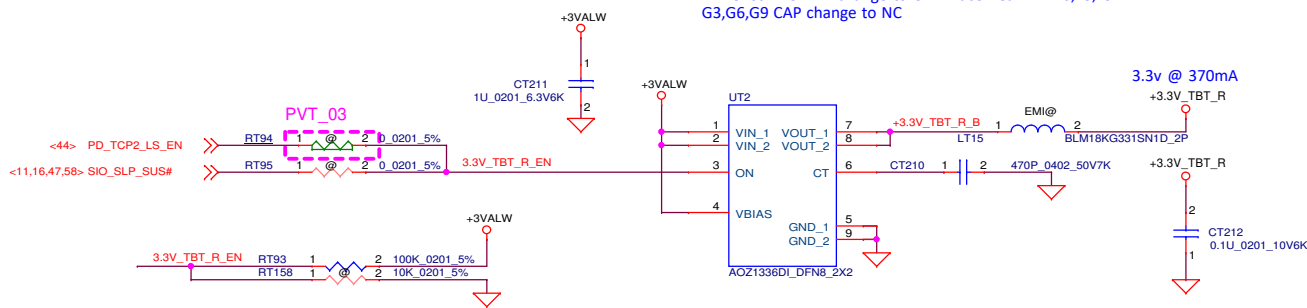
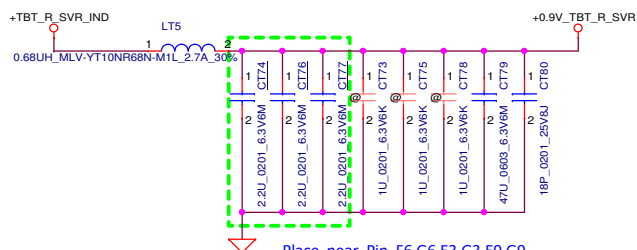
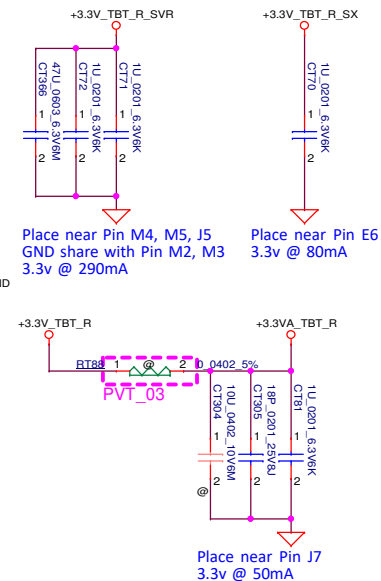
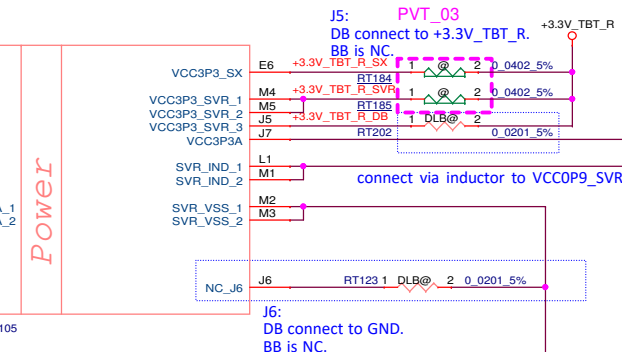
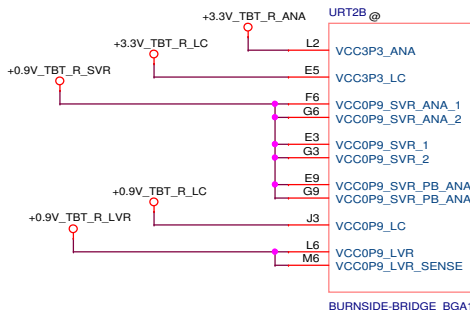
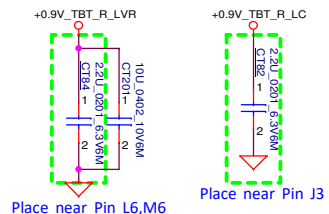
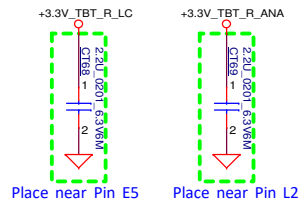
(A4) DG\_FLASH\_SHARE\_EN (IPU):   
'0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.   
'1' - Flash is shared between 2 Re-timers.

(A5) DG\_FLASH\_MSTR\_SLV (IPU):   
'0' - Set Re-timer to be Slave on shared flash SPI I/F.   
'1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG\_POC\_GPIO0:   
'0' -Reserved for debug   
'1' -Indication to S0 state for Re-timer

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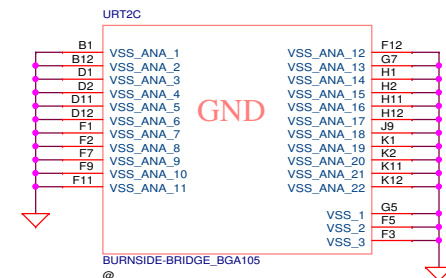




BB ref sch p.6 note  
DG\_P1\_PWR\_GATE\_EN:

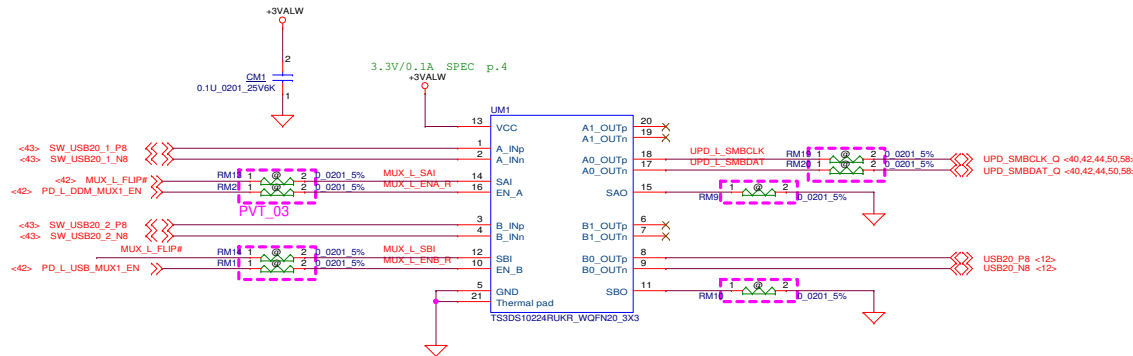
For PD based systems, DG\_P1\_PWR\_GATE\_EN should be output from PD.

For TCPC based systems, DG\_P1\_PWR\_GATE\_EN should be output from SOC/EC.

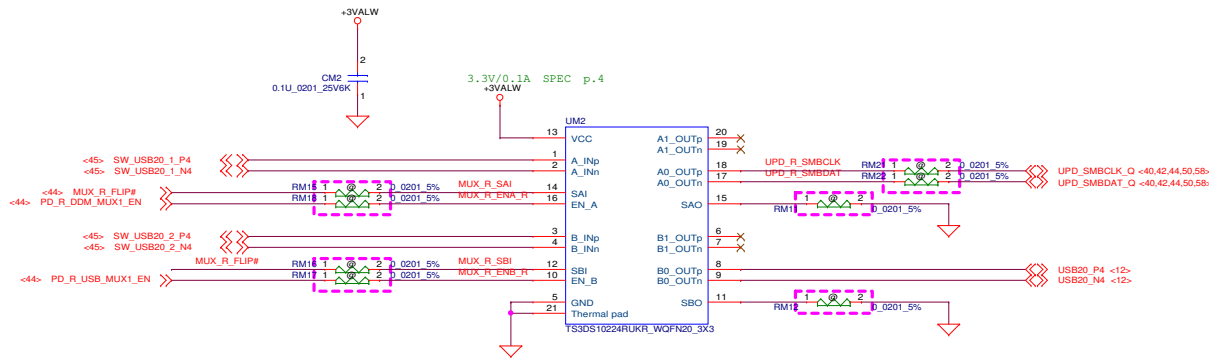


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				Size	Document Number
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# USB2/I2C MUXES\_L



# USB2/I2C MUXES\_R



ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	-	-
10	-	-	Hi-Z	Hi-Z
11	-	-	-	-

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	-	-	-
0001	INB	-	-	INA
0010	INB	-	INB	-
0011	INB	-	-	INB
0100	-	INB	INA	-
0101	-	INB	-	INA
0110	-	INB	INB	-
0111	-	INB	-	INB
1000	INA	-	INA	-
1001	INA	-	-	INA
1010	INA	-	INB	-
1011	INA	-	-	INB
1100	-	INA	INA	-
1101	-	INA	-	INA
1110	-	INA	INB	-
1111	-	INA	-	INB

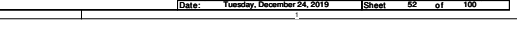
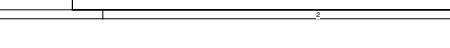
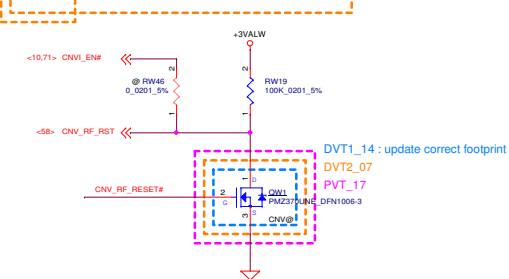
Channel	INA	INB
Signal Name	TOP	BOT

					I2C	USB		
ENA	ENB	SAI	SBI	SAO	OUTA0	OUTB0	Mux Functional Mode	PD Controller W/DDM
0	1	-	0	-	Hi-Z	TOP	-	USB only on TOP
0	1	-	1	-	Hi-Z	BOT	-	USB only on BOT
1	1	0	0	0	BOT	TOP	Crosspoint Switch	USB on TOP W/DDM
1	1	1	1	0	TOP	BOT	Crosspoint Switch	USB on BOT W/DDM

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				Size	Document Number
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				Tuesday, December 24, 2019	0.1 (X00)
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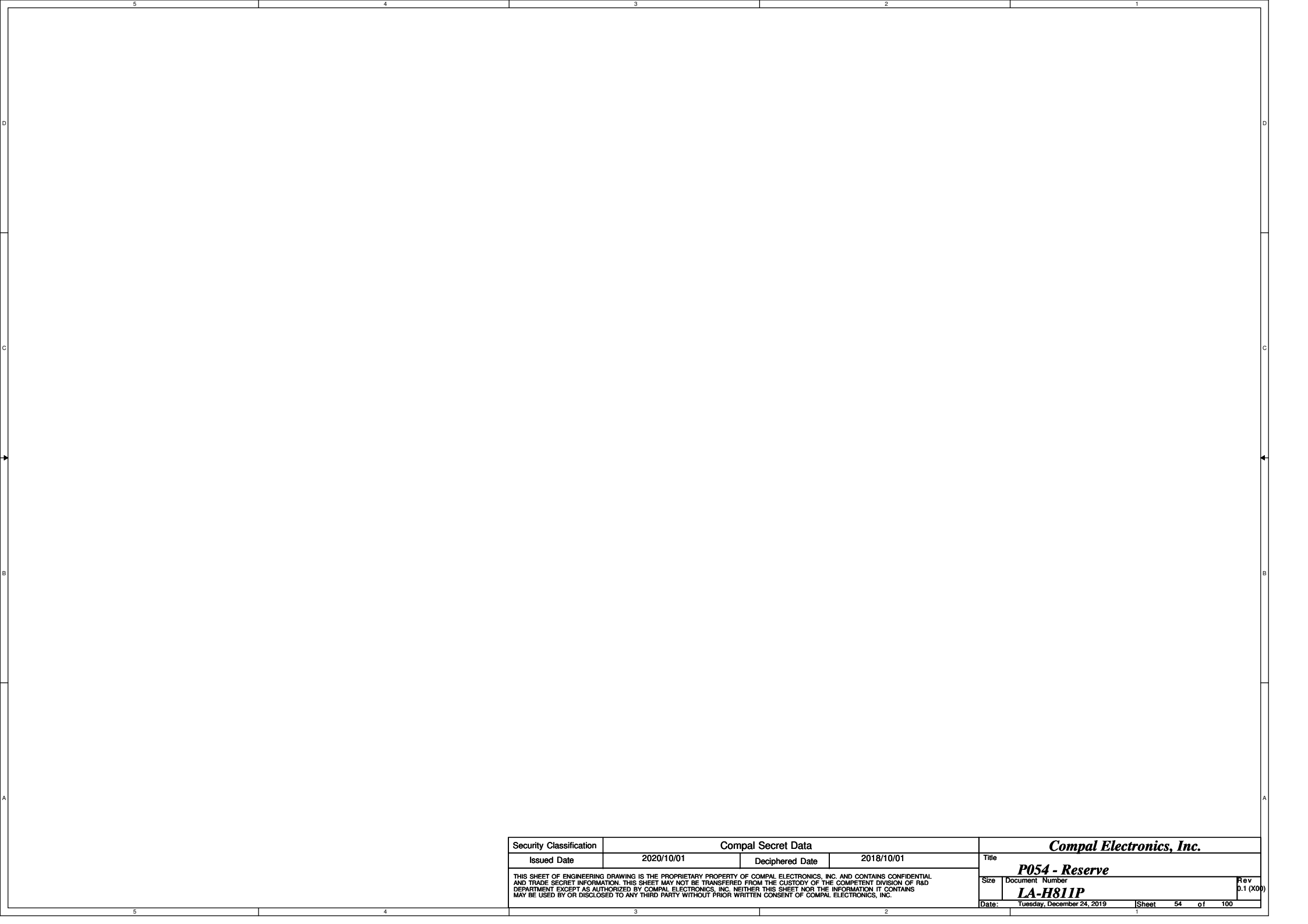
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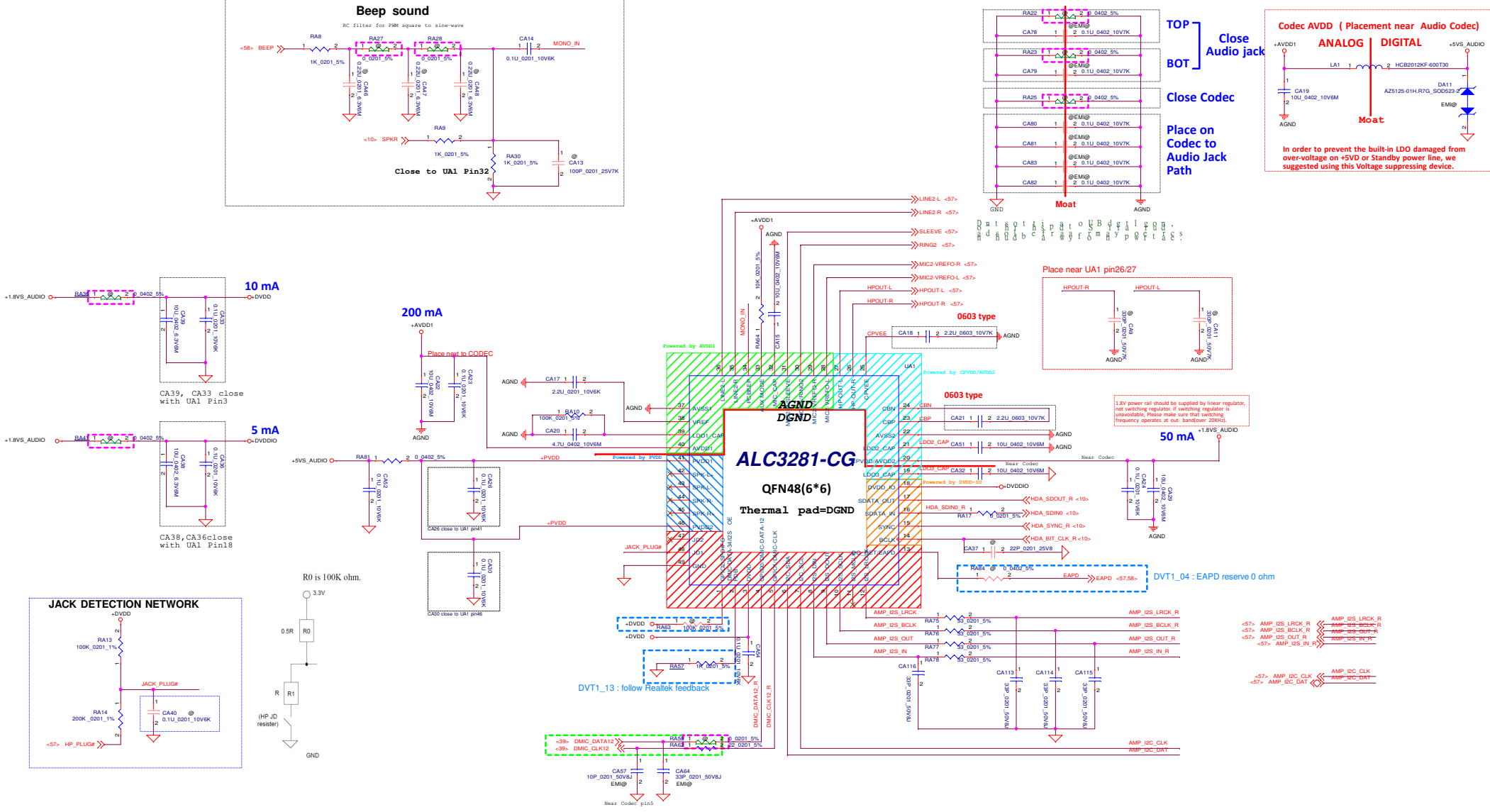
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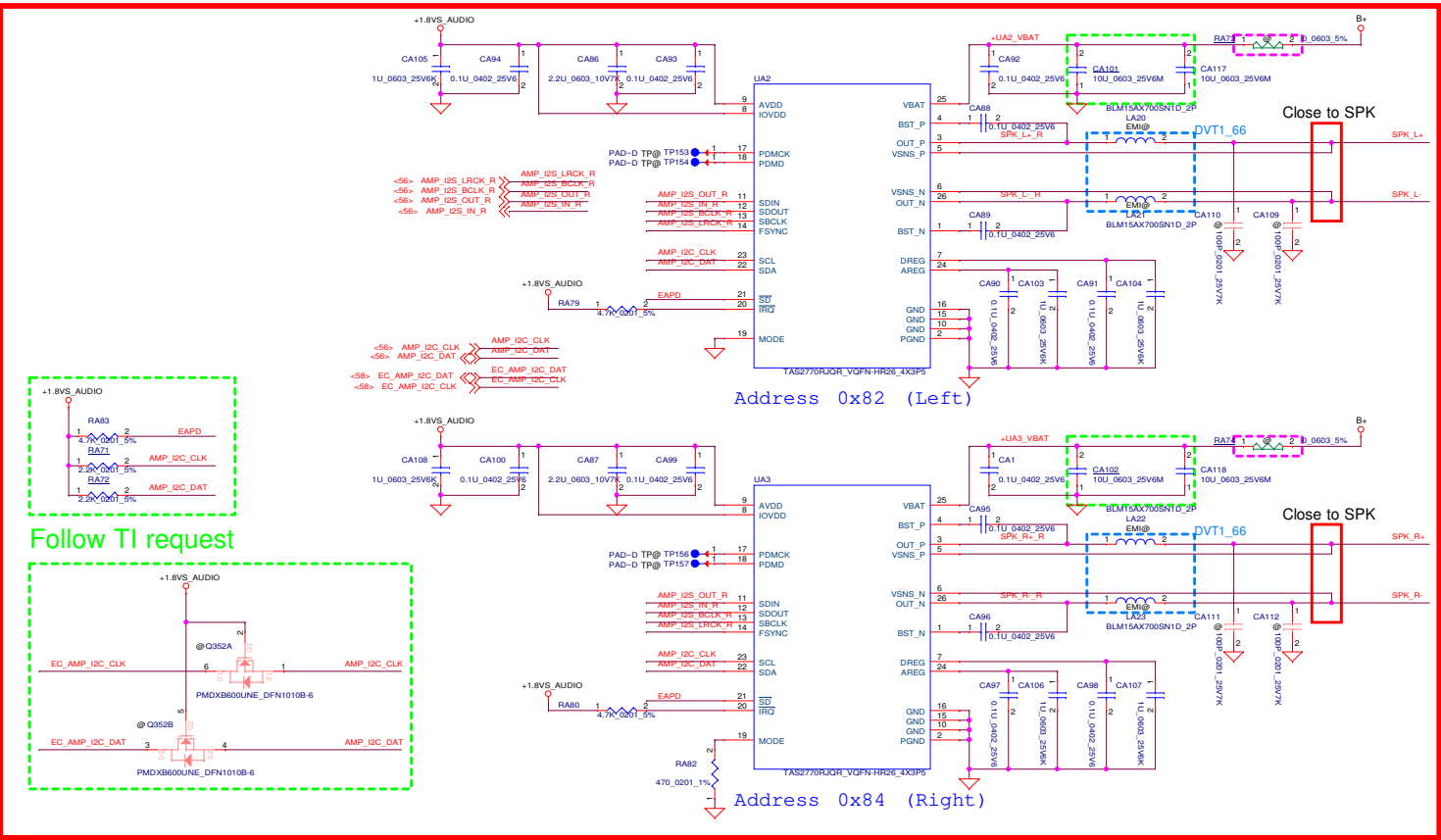
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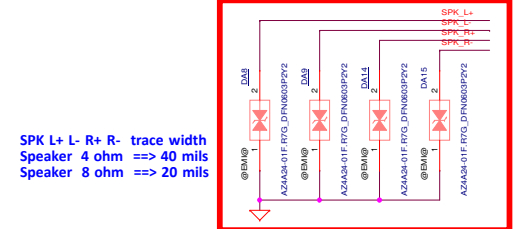
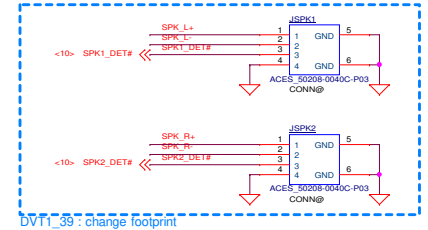
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		Date: Tuesday, December 24, 2019			Sheet 55 of 100
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				P055 - Reserve	
				LA-H811P	



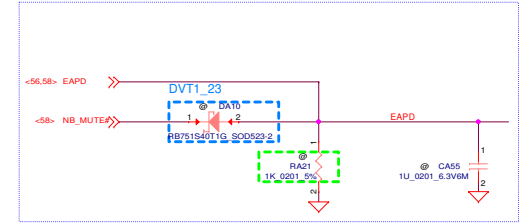




## Int. Speaker Conn.



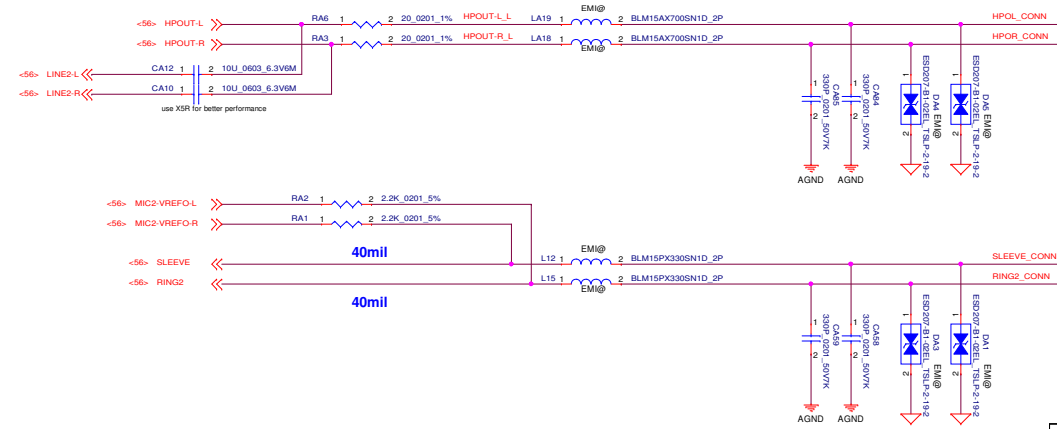
Need up to 15+V, check with EMC



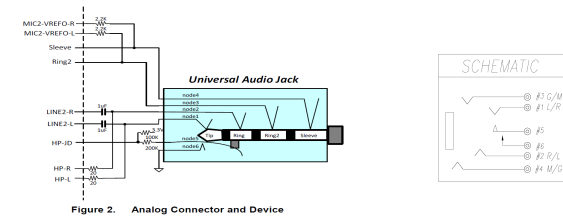
PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.  
LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

change RA6/RA3 to 5.6 ohm to meet Dell Grade A headphone output power > 25 mW setting

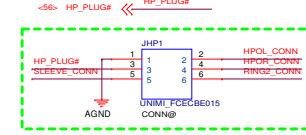
## Universal Audio Jack



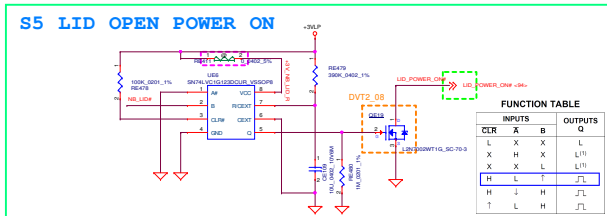
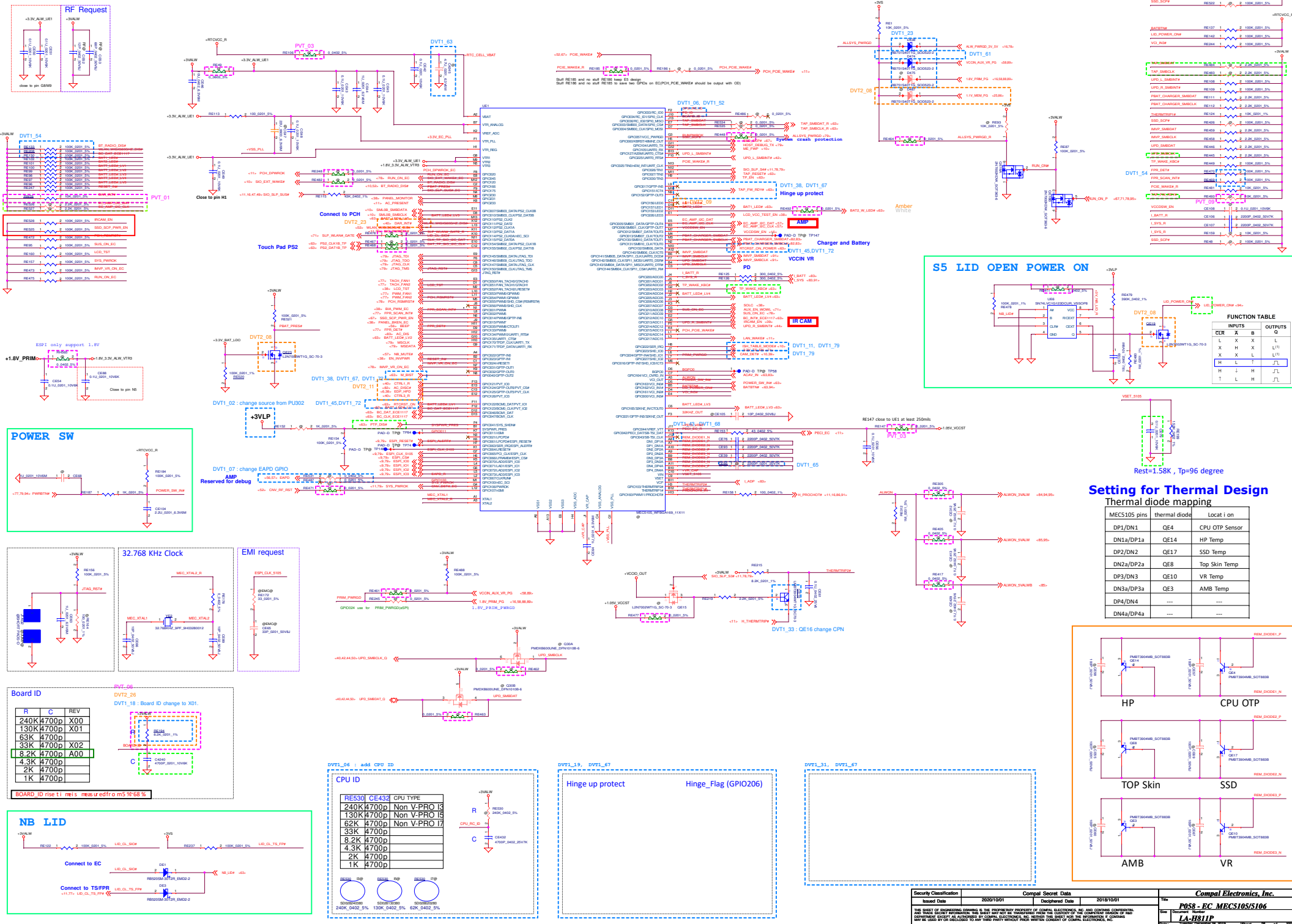
## Universal Audio Jack CONN



## Contact with PC BEAN



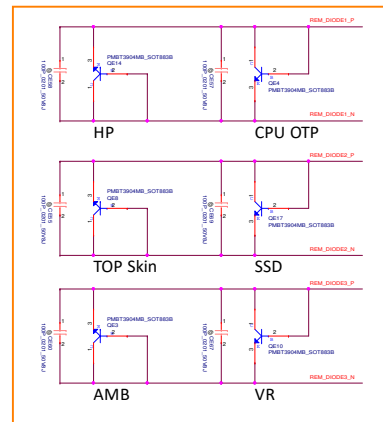
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Issued Date	2020/10/01	Deciphered Date	2018/10/01
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FUNCTION TABLE			
INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	L	H
L	L	H	H

### Setting for Thermal Design

MECS105 pins	thermal diode	Locat i on
DP1/DN1	QE4	CPU OTP Sensor
DN1a/DP1a	QE14	HP Temp
DP2/DN2	QE17	SSD Temp
DN2a/DP2a	QE18	Top Skin Temp
DP3/DN3	QE10	VR Temp
DN3a/DP3a	QE3	AMB Temp
DP4/DN4	---	---
DN4a/DP4a	---	---



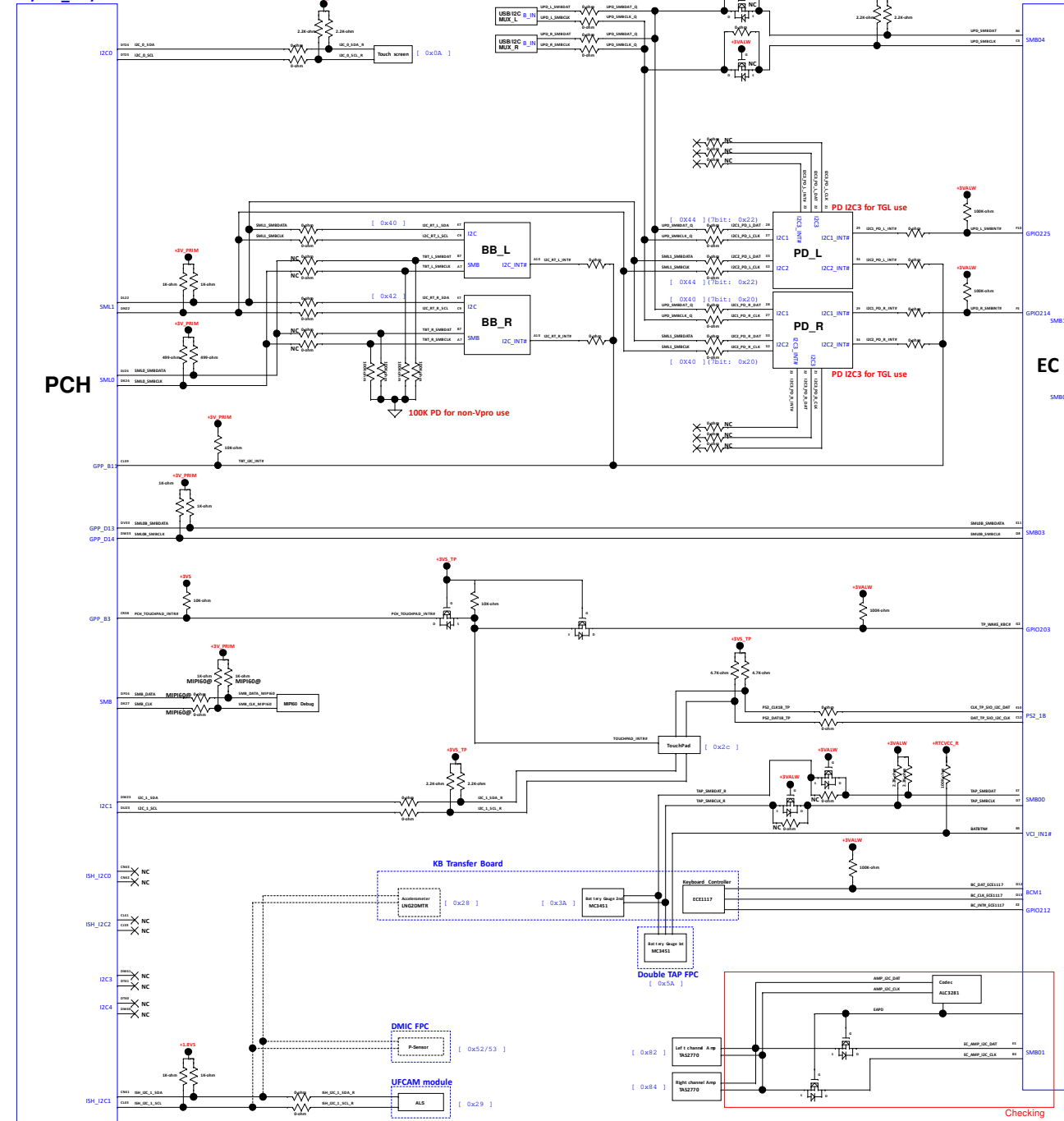


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				Size	Document Number
				LA-H811P	
Date:		Tuesday, December 24, 2019		Sheet	59 of 100
				Rev	0.1 (X00)

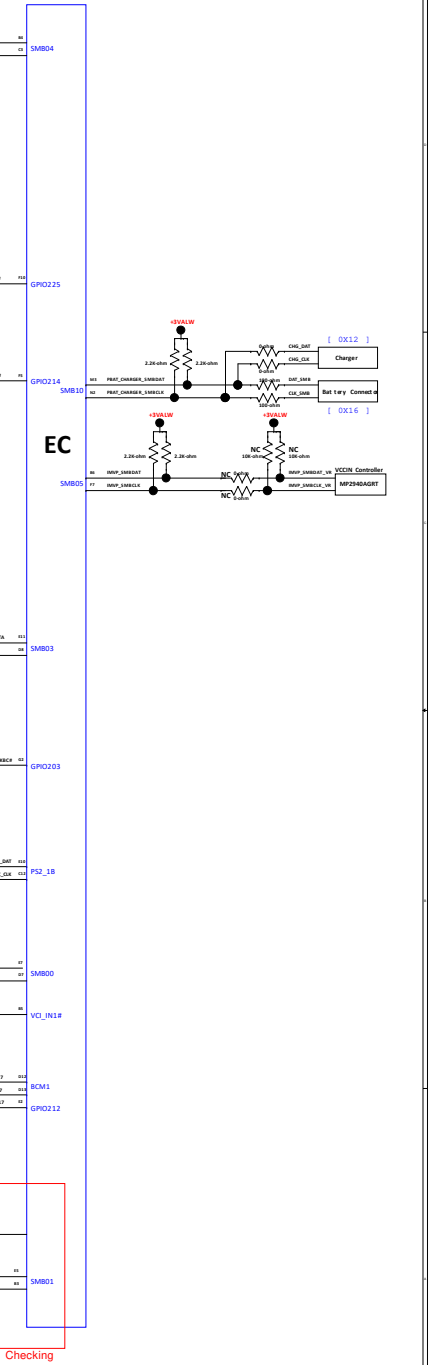


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				Sheet	60 of 100
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## I2C/ISH\_I2C/SML



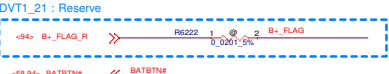
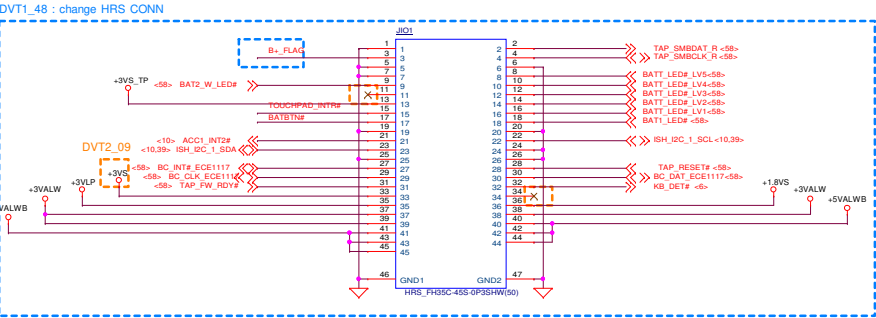
## SMBus



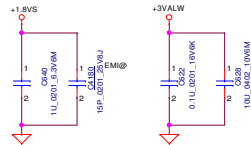


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					Size	Document Number			Rev
					Date:	Tuesday, December 24, 2019	Sheet	62	of

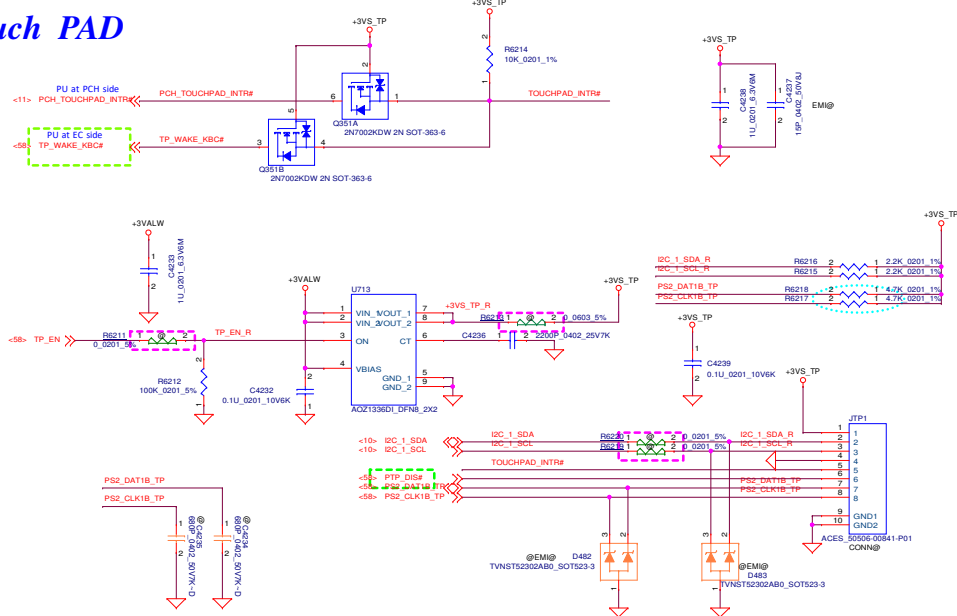
KB Controller & TP transfer Conn



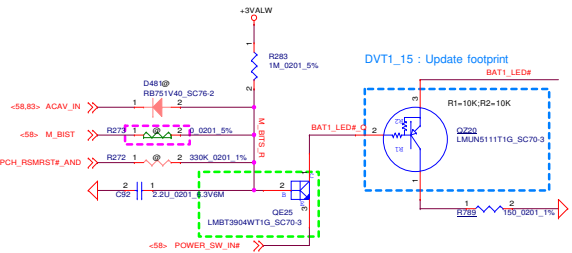
11 CONNECTOR:  
TOUCHPAD DATA TO SYSTEM PIN ASSIGNMENTS:  
PIN 1 = VDD  
PIN 2 = IC DATA  
PIN 3 = IC CLK  
PIN 4 = GND  
PIN 5 = ATTN  
PIN 6 = PTP DISABLE (PDIOL, CLOSE LID)  
PIN 7 = PS2 DATA  
PIN 8 = PS2 CLK



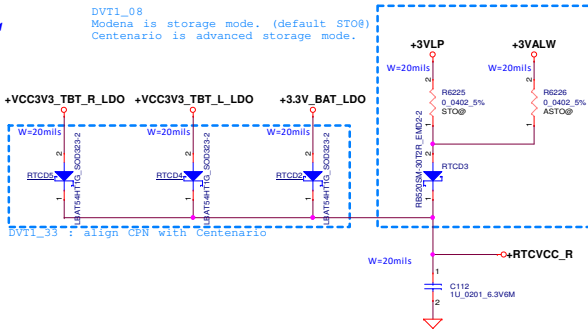
Touch PAD



M-BIST



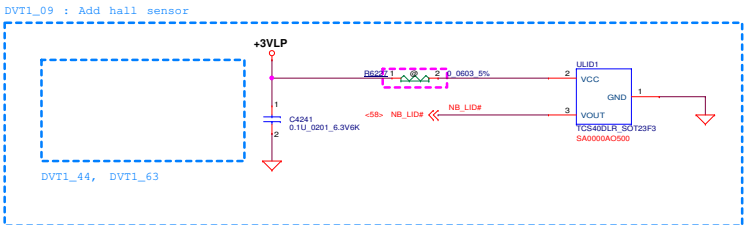
RTC



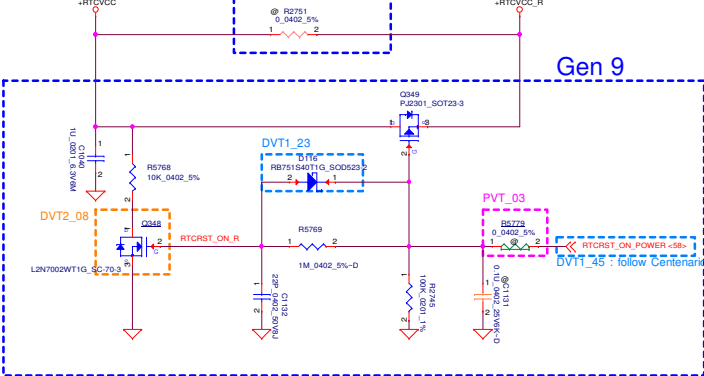
For manufacturer process use only



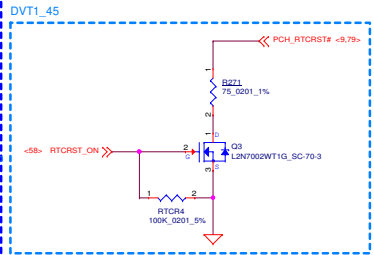
Hall Sensor



Gen 8 reserved



Gen 9





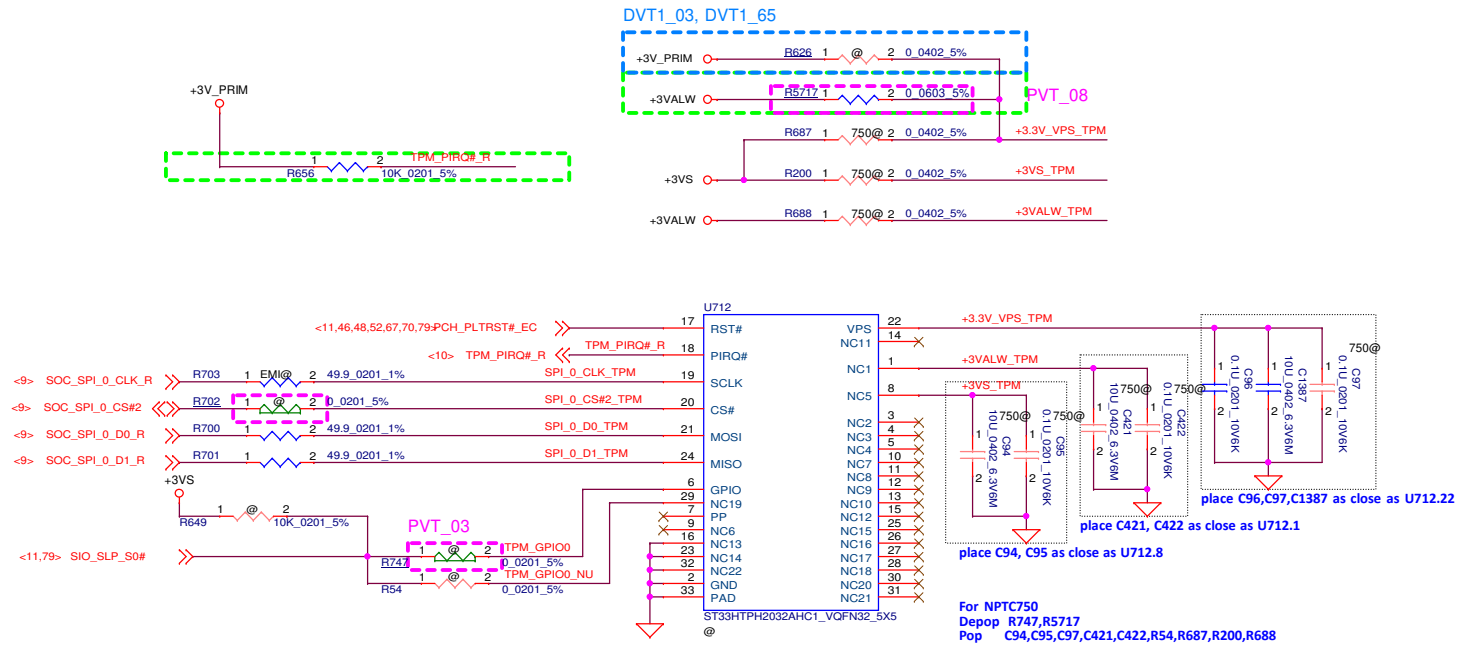
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Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P064 - Reserve
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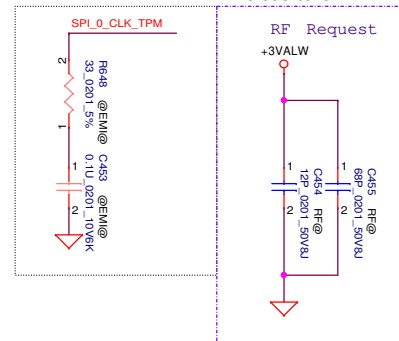


Security Classification		Compal Secret Data		Compal Electronics, Inc.					
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# For ST/Nuvoton TPM



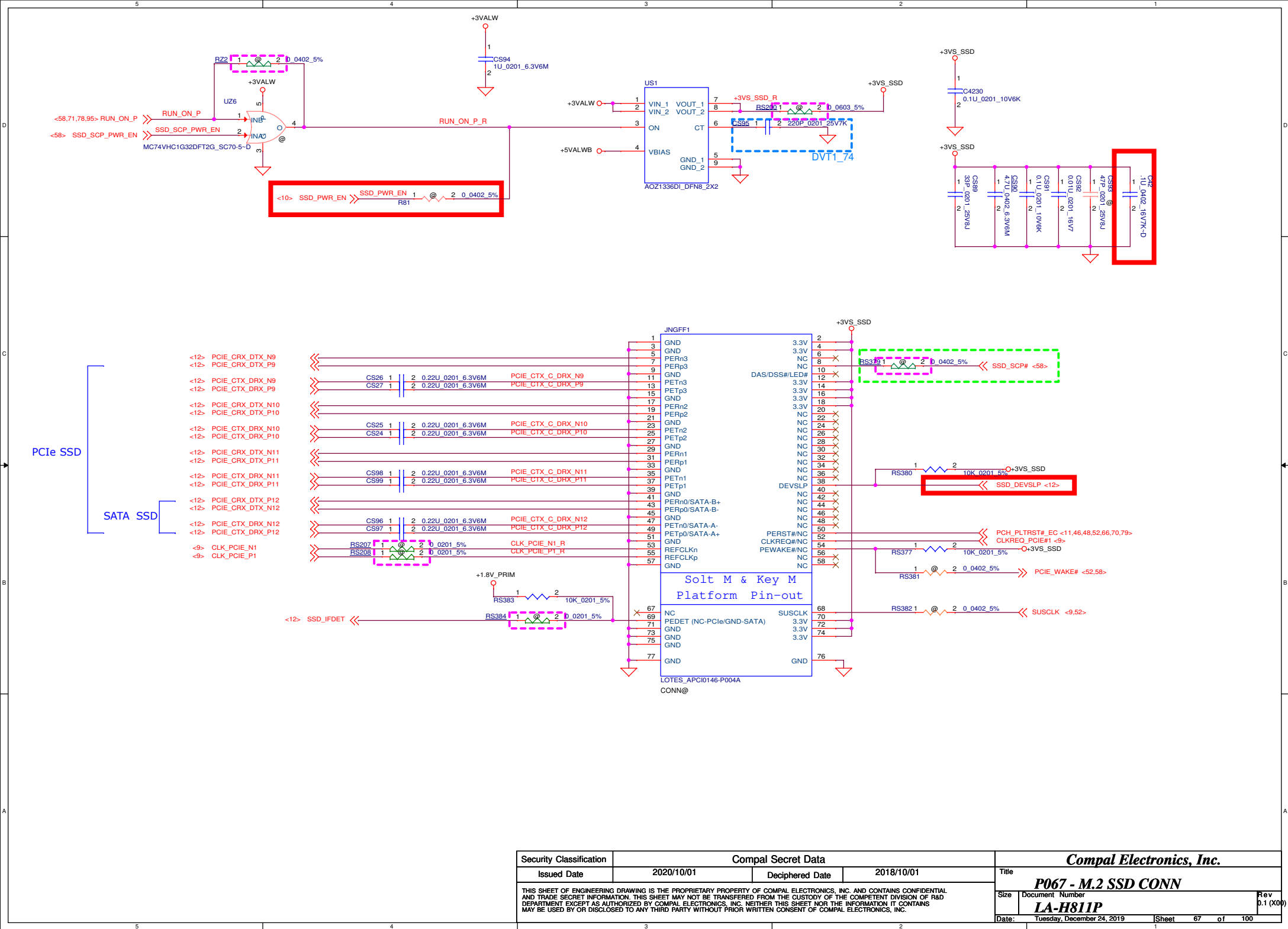
## Close to U712



Pin number	1	2	6	8	16	17	18	19	20	21	22	23	24	29
Chip	1	2	6	8	16	17	18	19	20	21	22	23	24	29
ST33	NC	GND	GPIO0	NC	NC	RESET	PIRQ	SCLK	SCS	MOSI	GPIO0	NC	MISO	NC
NPCT750	VDD	NC	NC	GPIO0	GND	RESET	PIRQ	SCLK	SCS	MOSI	GPIO0	NC	MISO	NC

VSB Standby Power Supply. The VALW power rail 3.3V  
 VHI0 Host Interface Power Supply 3.3V  
 VPS: Power Supply 3.3V  
 NPCT750: GPIO0 can be used as a backup option for entering Low-Power mode.

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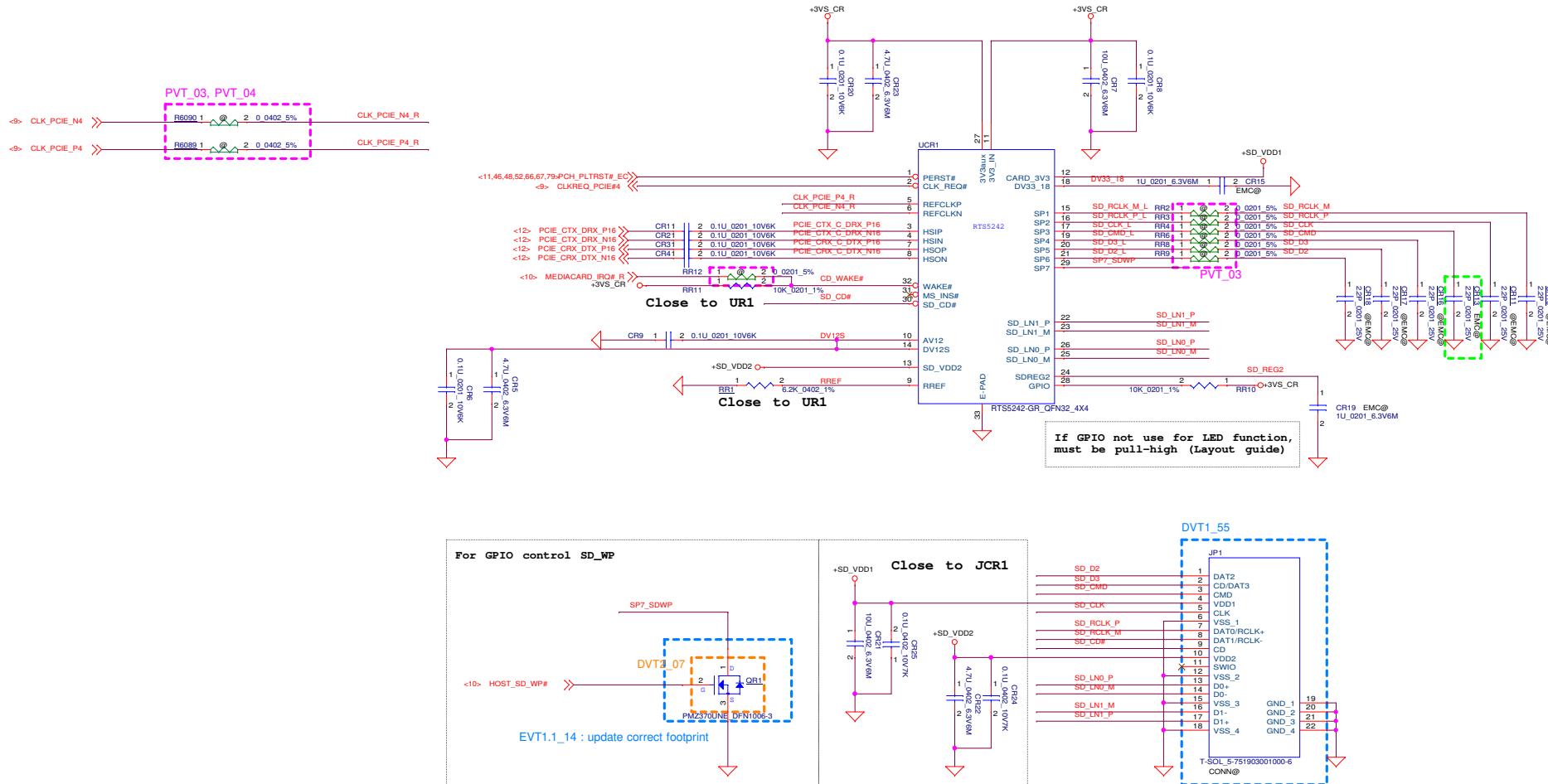
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Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P068 - Reserve
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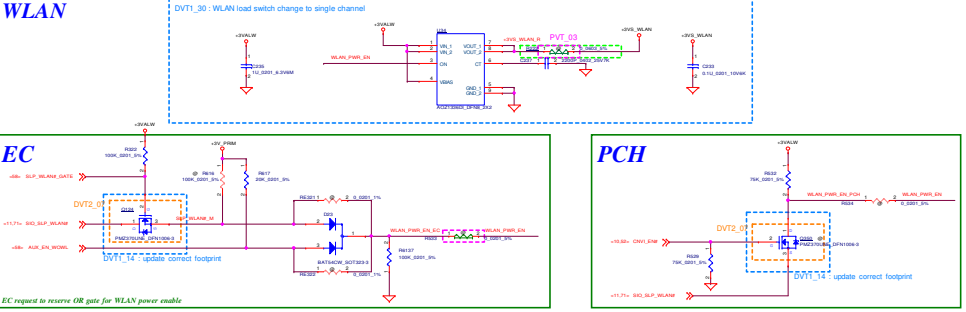
# Card Reader

- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
  - Bulk capacitor for Card\_3V3 place closed to flash card socket.
  - Bulk capacitor for 3V3\_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.

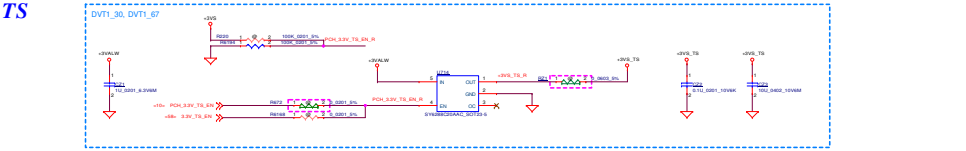


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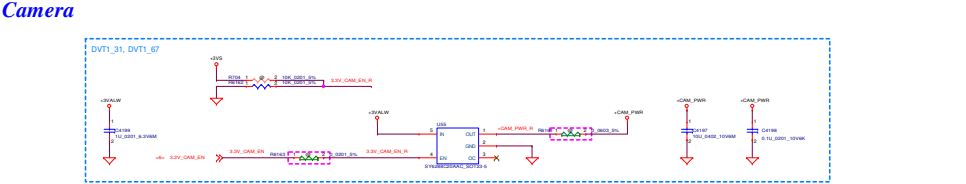
WLAN



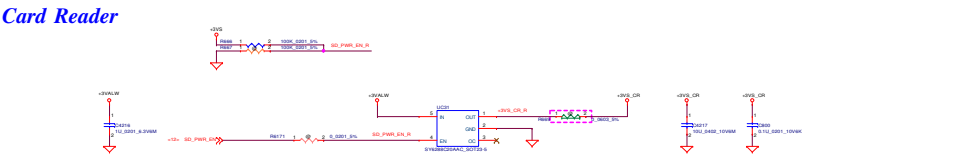
TS



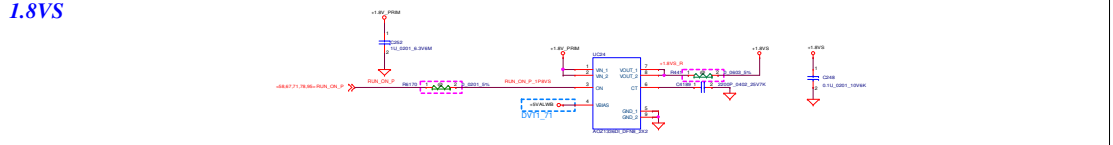
Camera



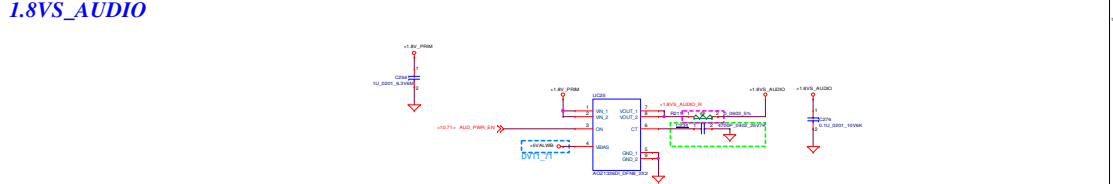
Card Reader



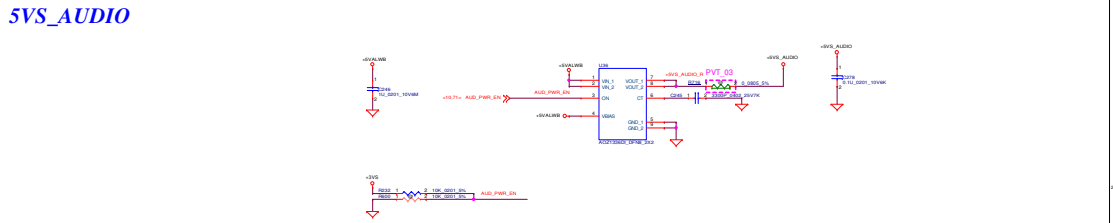
1.8VS



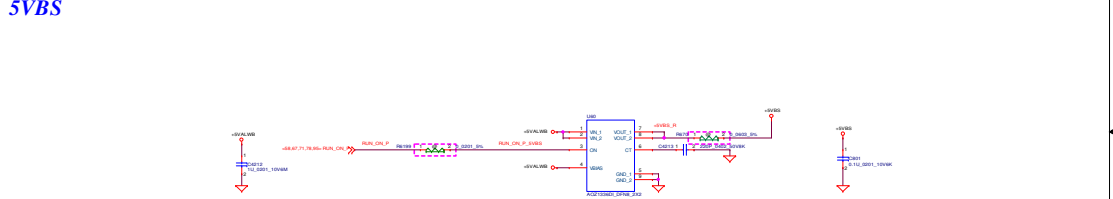
1.8VS\_AUDIO



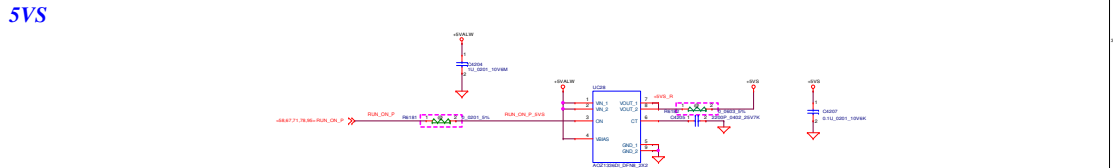
5VS\_AUDIO



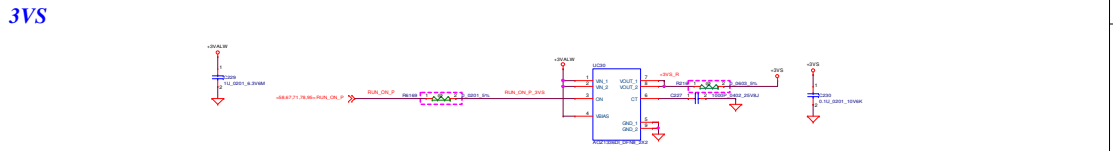
5VBS

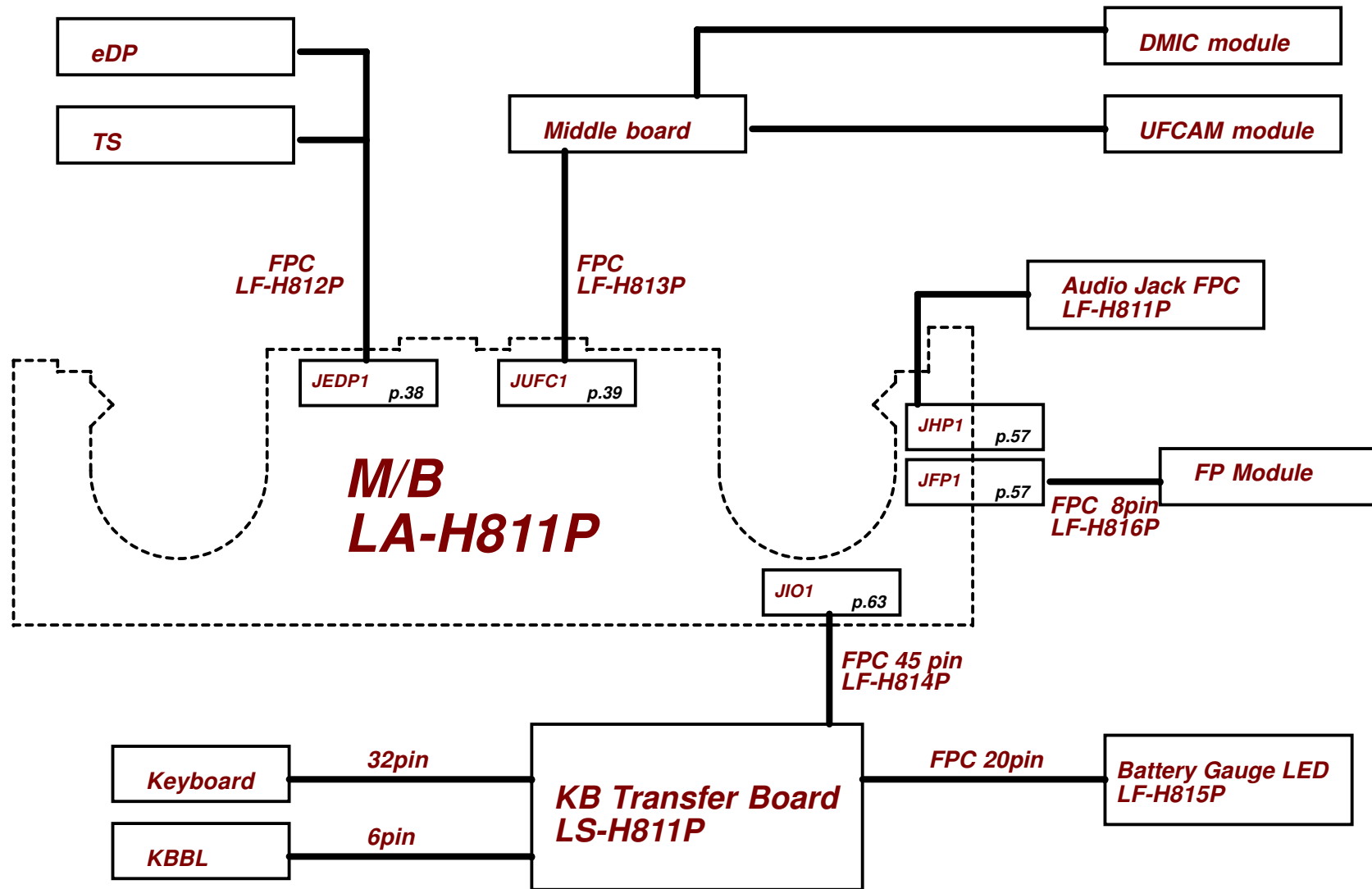


5VS



3VS



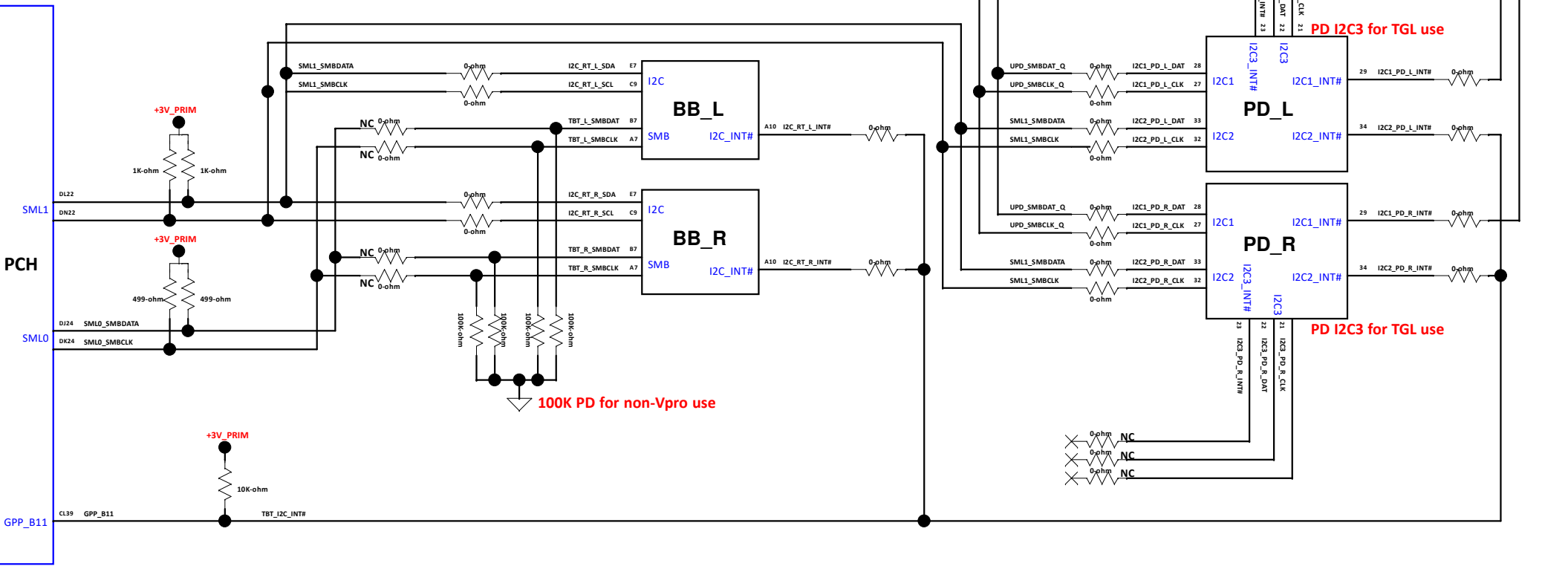


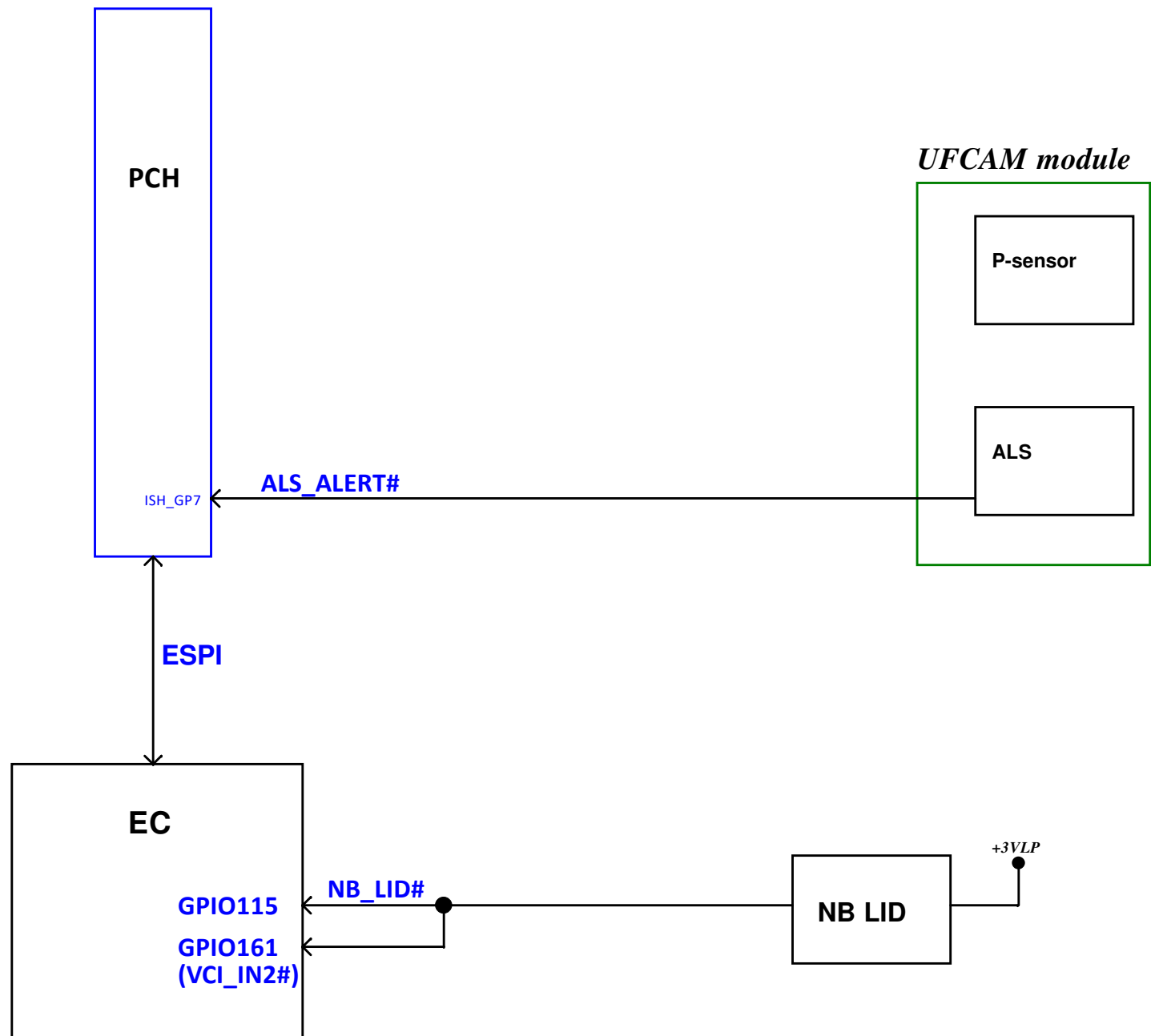
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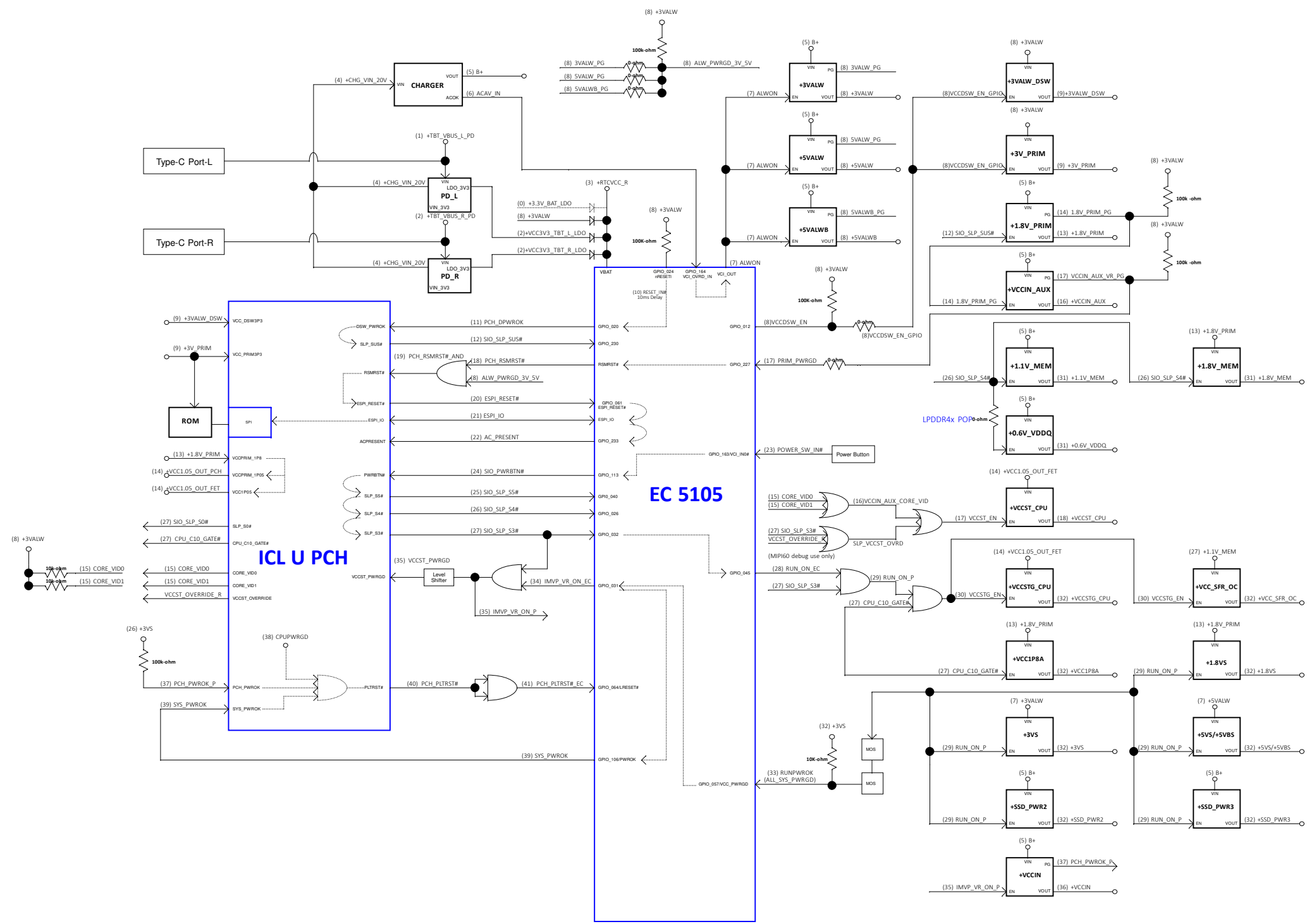


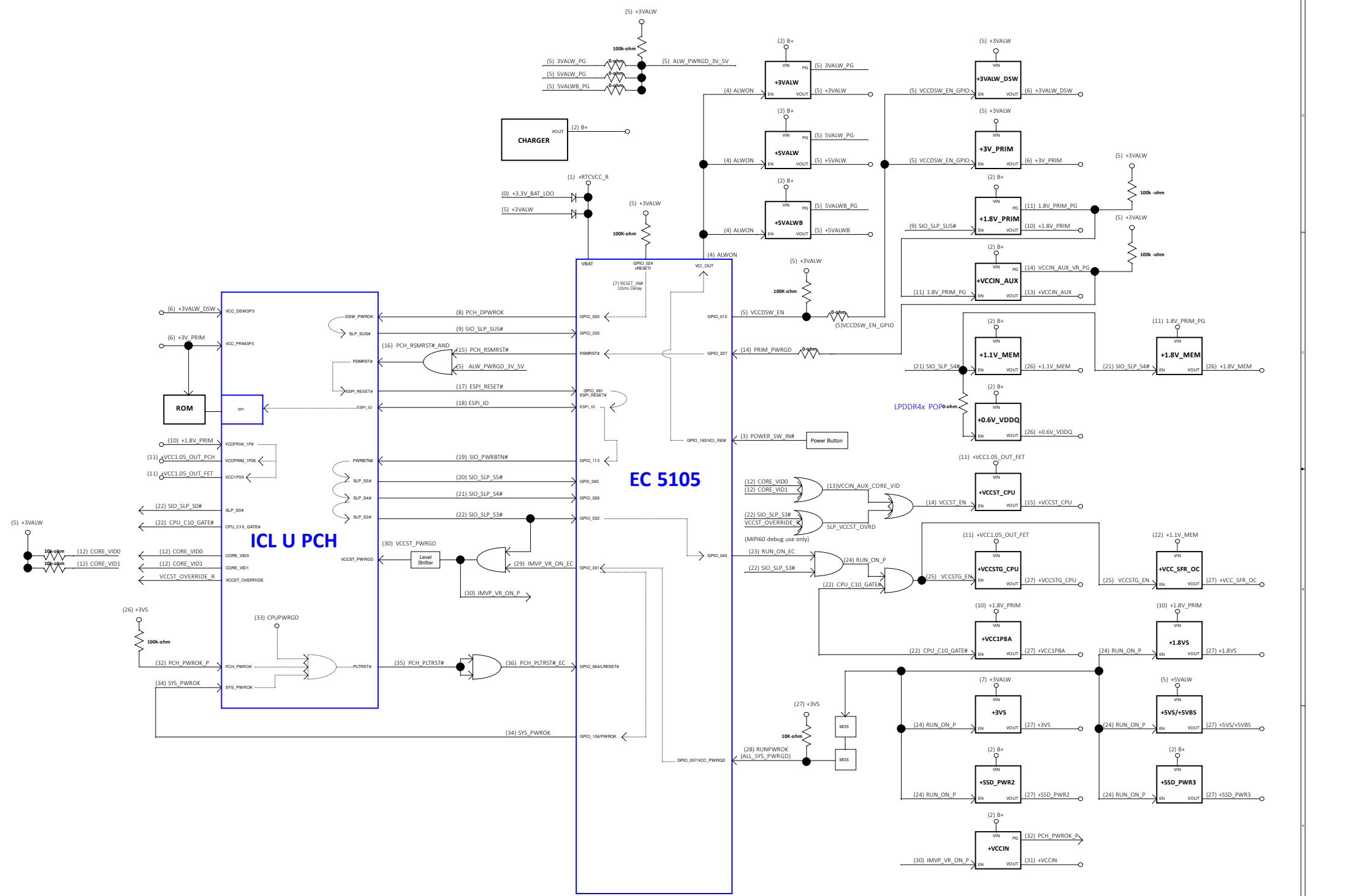
To LEFT Type-C Connector

To RIGHT Type-C Connector



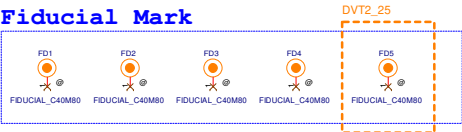




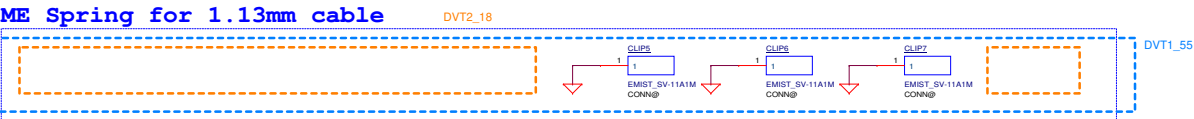


Screw Hole

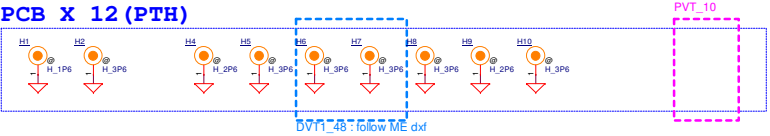
Fiducial Mark



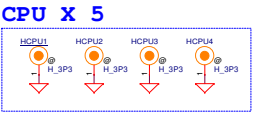
ME Spring for 1.13mm cable



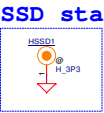
PCB X 12 (PTH)



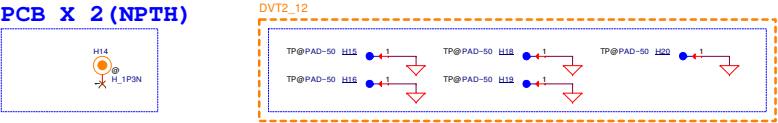
CPU X 5



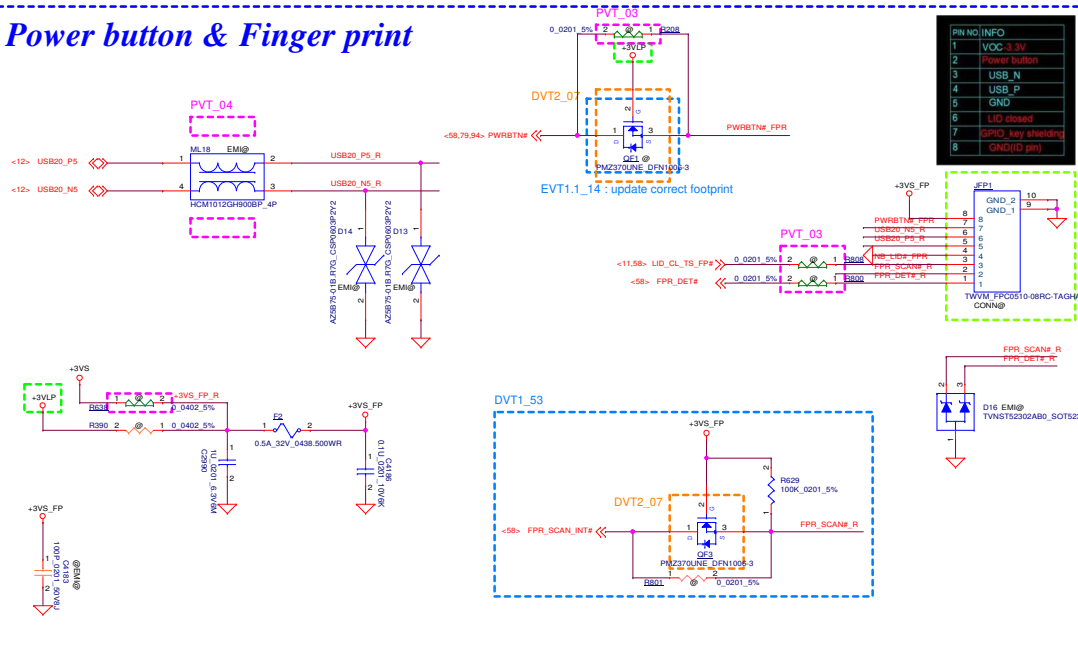
SSD stand-off



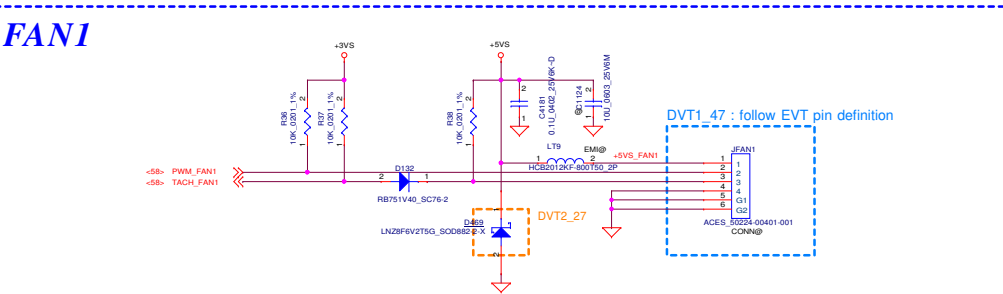
PCB X 2 (NPTH)



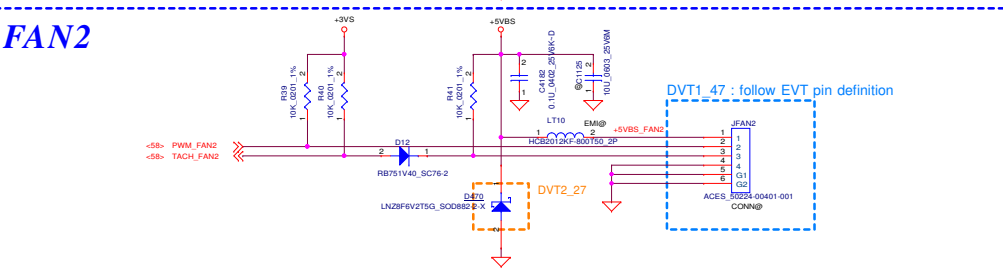
Power button & Finger print



FAN1

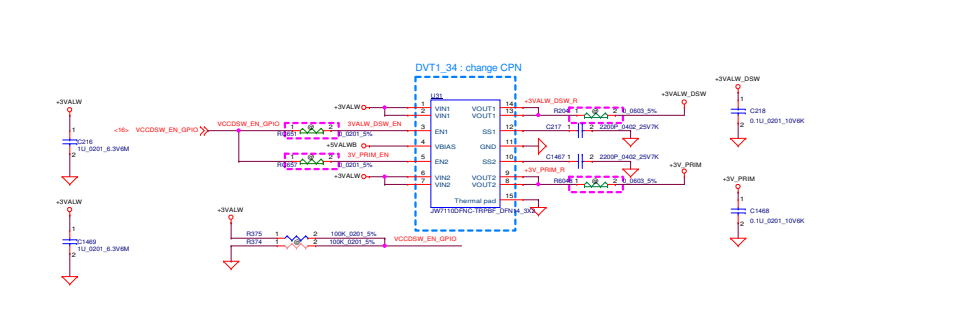


FAN2

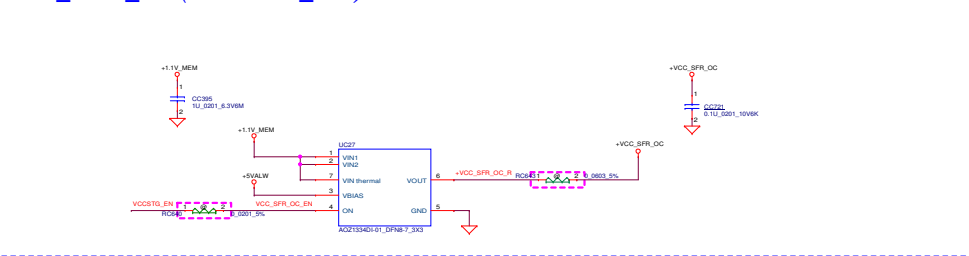


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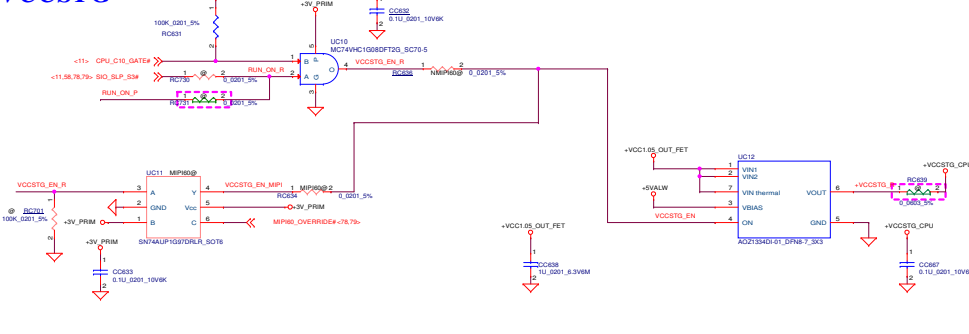
**+3VALW\_DSW&+3V\_PRIM**



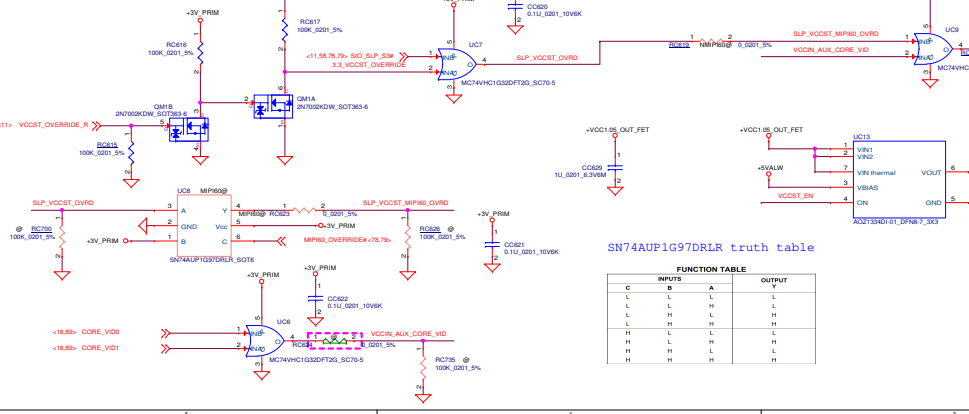
**VCC\_SFR\_OC(VCCPLL\_OC)**



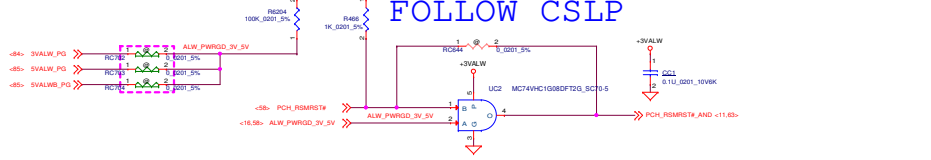
**VCCSTG**



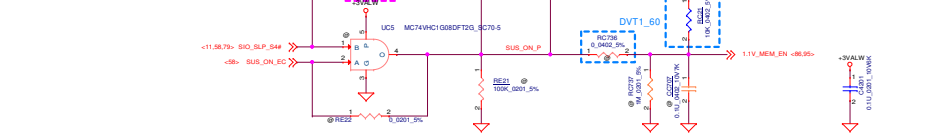
**VCCST**



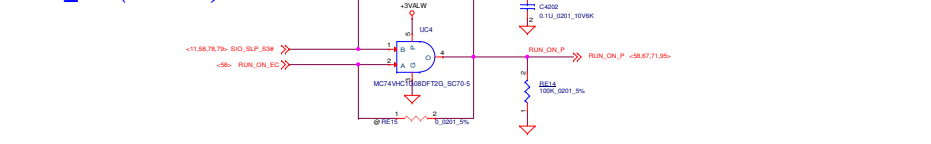
**RSMRST#**



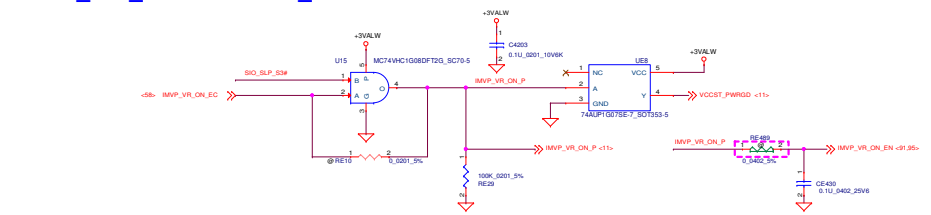
**SUS\_ON(DDR EN)**



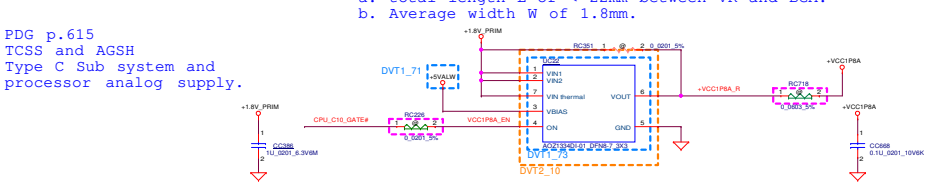
**RUN\_ON(VS EN)**



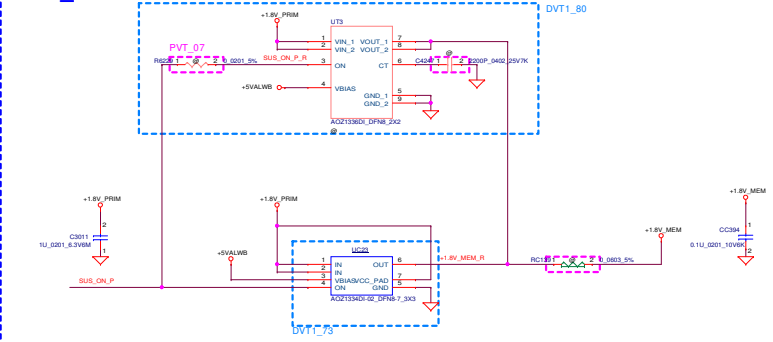
**IMVP\_VR\_ON&VCCST\_PWRGD**



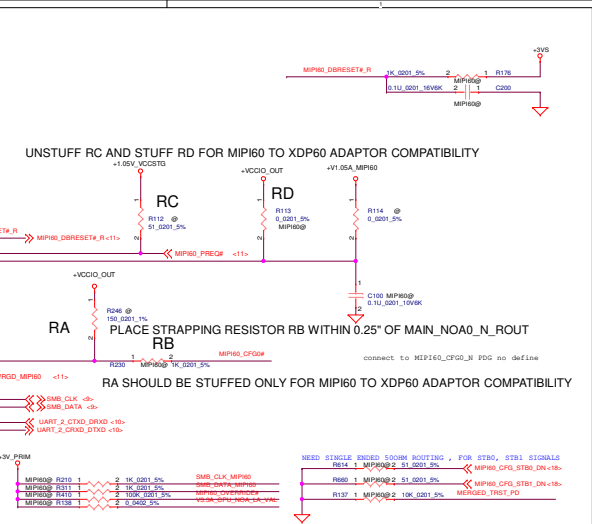
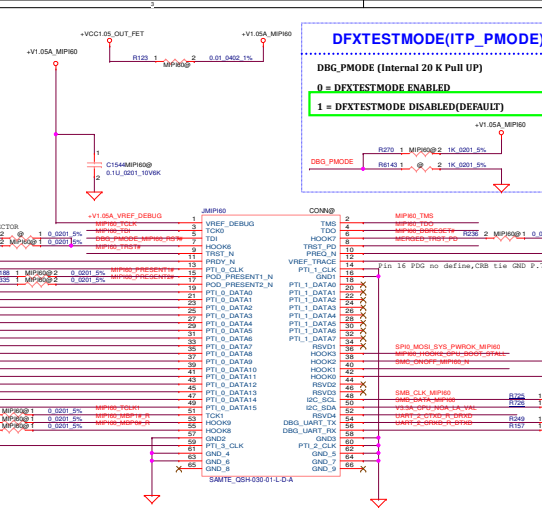
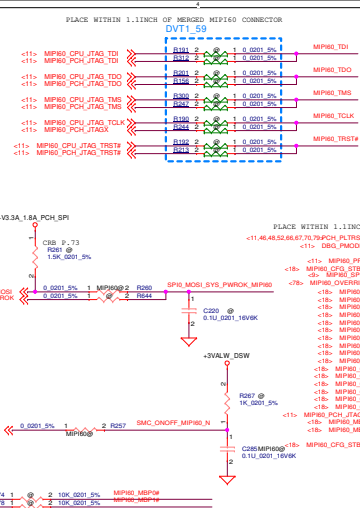
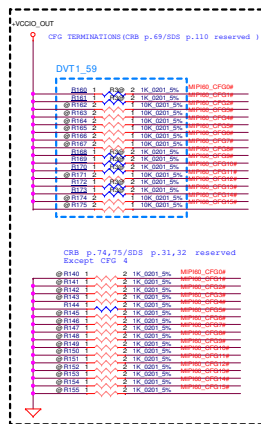
**+VCCIP8A**



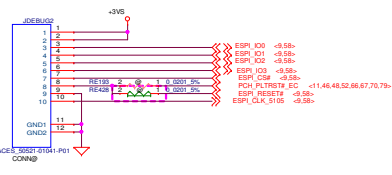
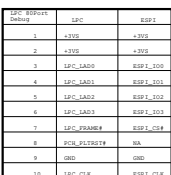
**+1.8\_MEM**



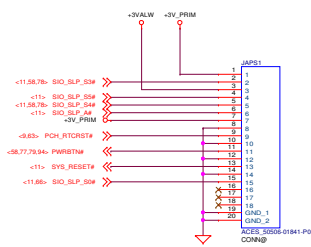
## MIPI 60



## JESPI



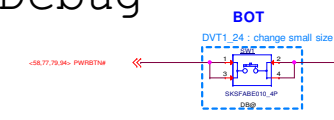
APS



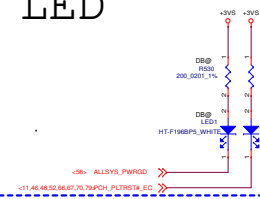
## BIOS UEFI Debug



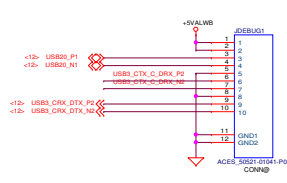
## Power Button Debug



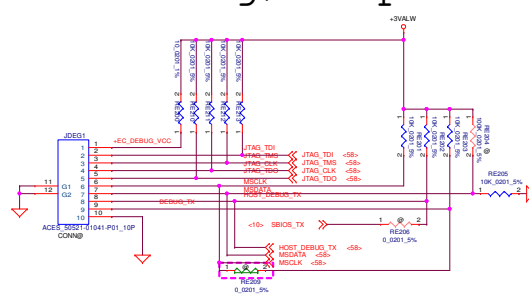
Debug LED



## DCI Debug



```
JDEG1
EC UART Debug/80 port
```



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Issued Date	2020/10/01	Deciphered Date	2018/10/01	
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	A	B	C	D	E
1					
2					
3					
4					

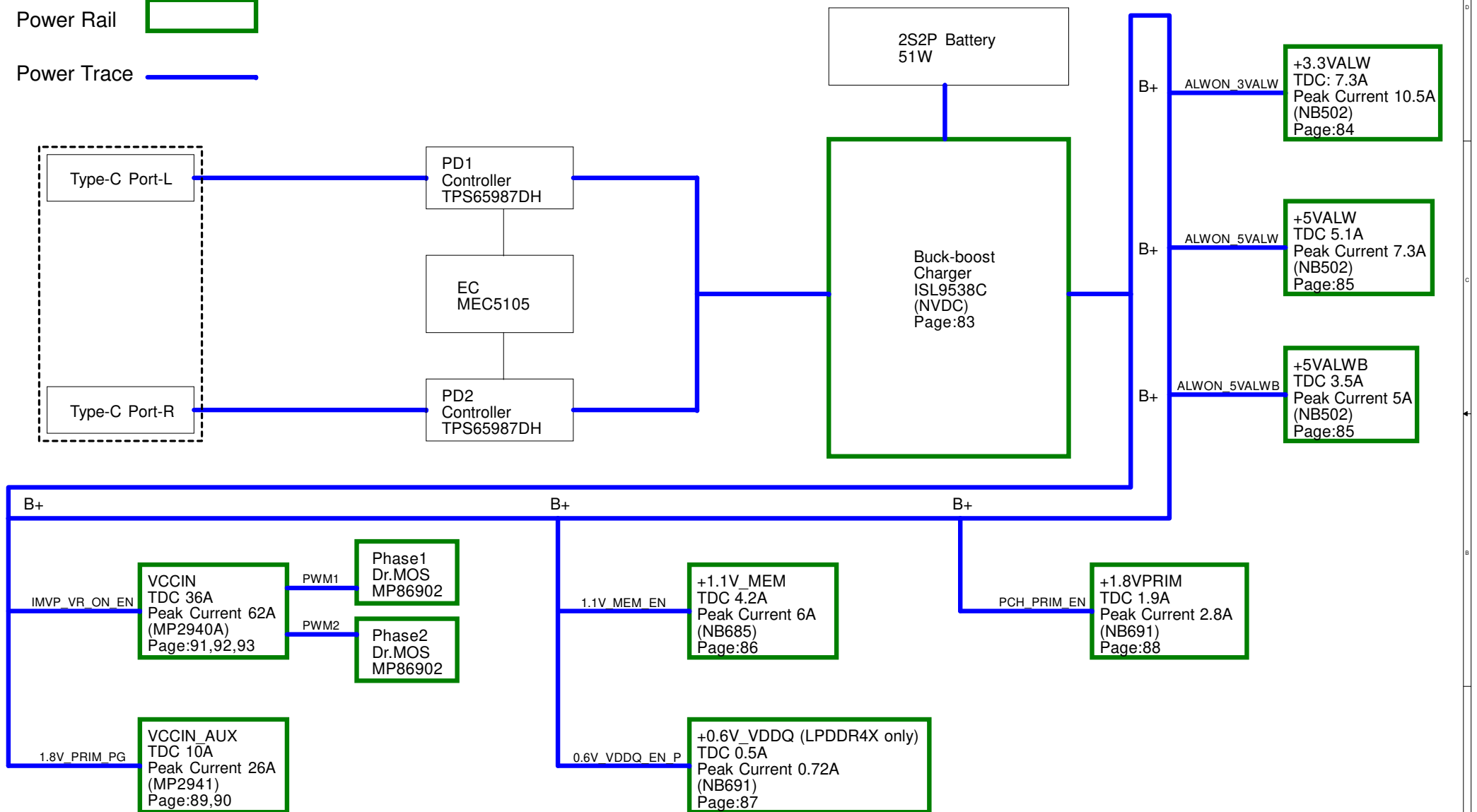
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Issued Date	2020/10/01	Deciphered Date	2018/10/01	Title	P080 - Reserved
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				LA-H811P	
				Date:	Tuesday, December 24, 2019
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## Modena POWER BLOCK DIAGRAM

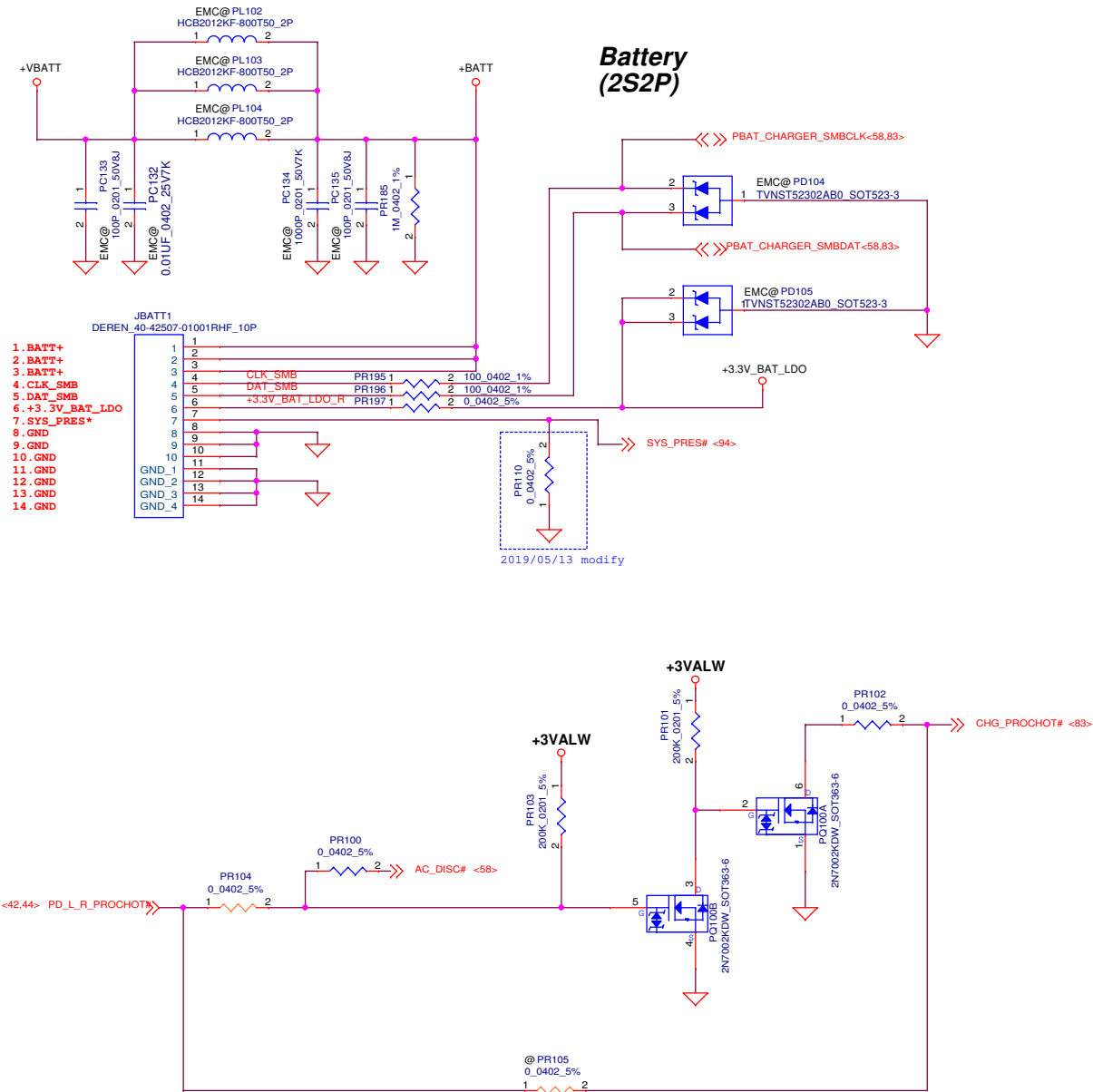
## Power Rail

## Power Trace

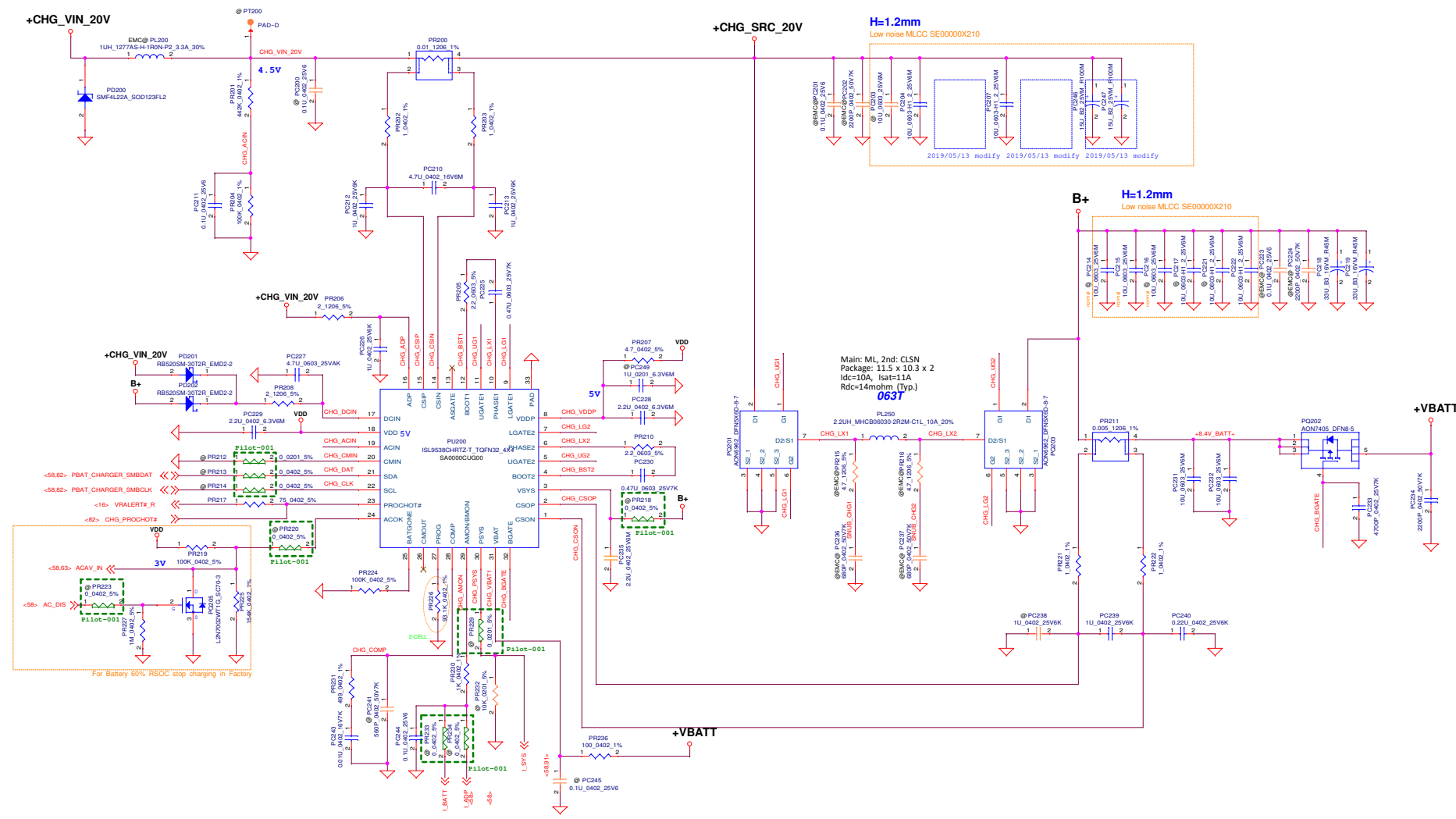


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Issued Date	2017/08/24		Deciphered Date	2017/08/24		Title
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				Size	Document Number	Rev
				LA-G172P		0.4 (202)
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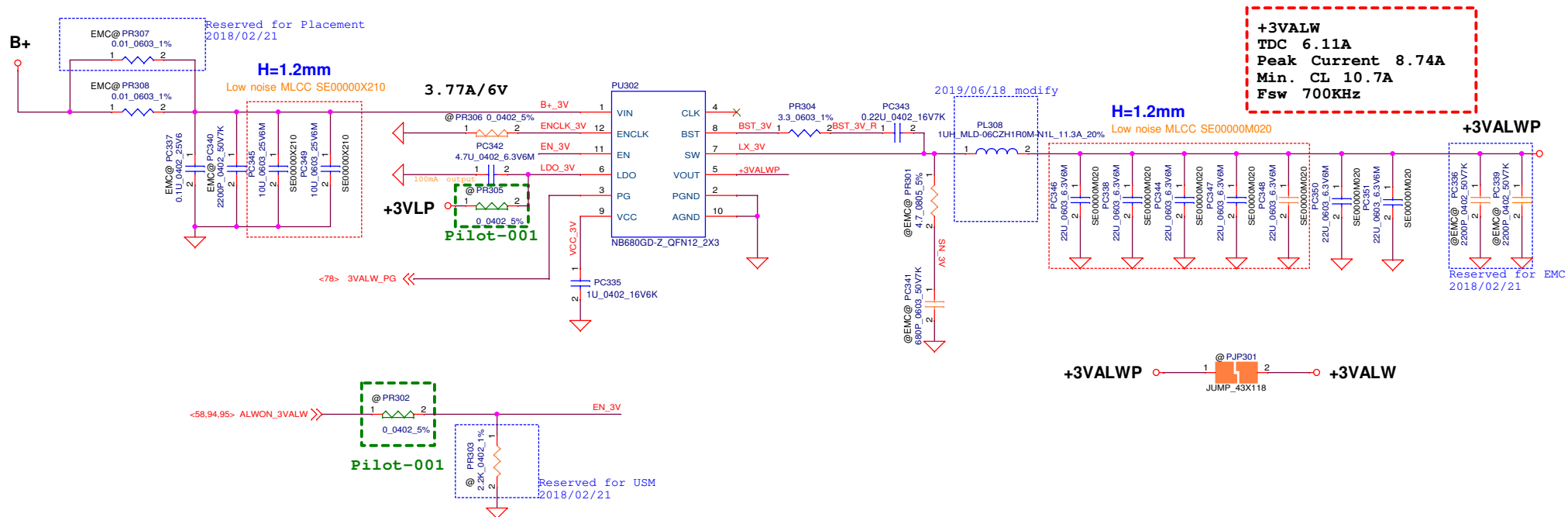
DCIN(37.1)



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				Sheet	82 of 100
				Rev	0.4 (202)

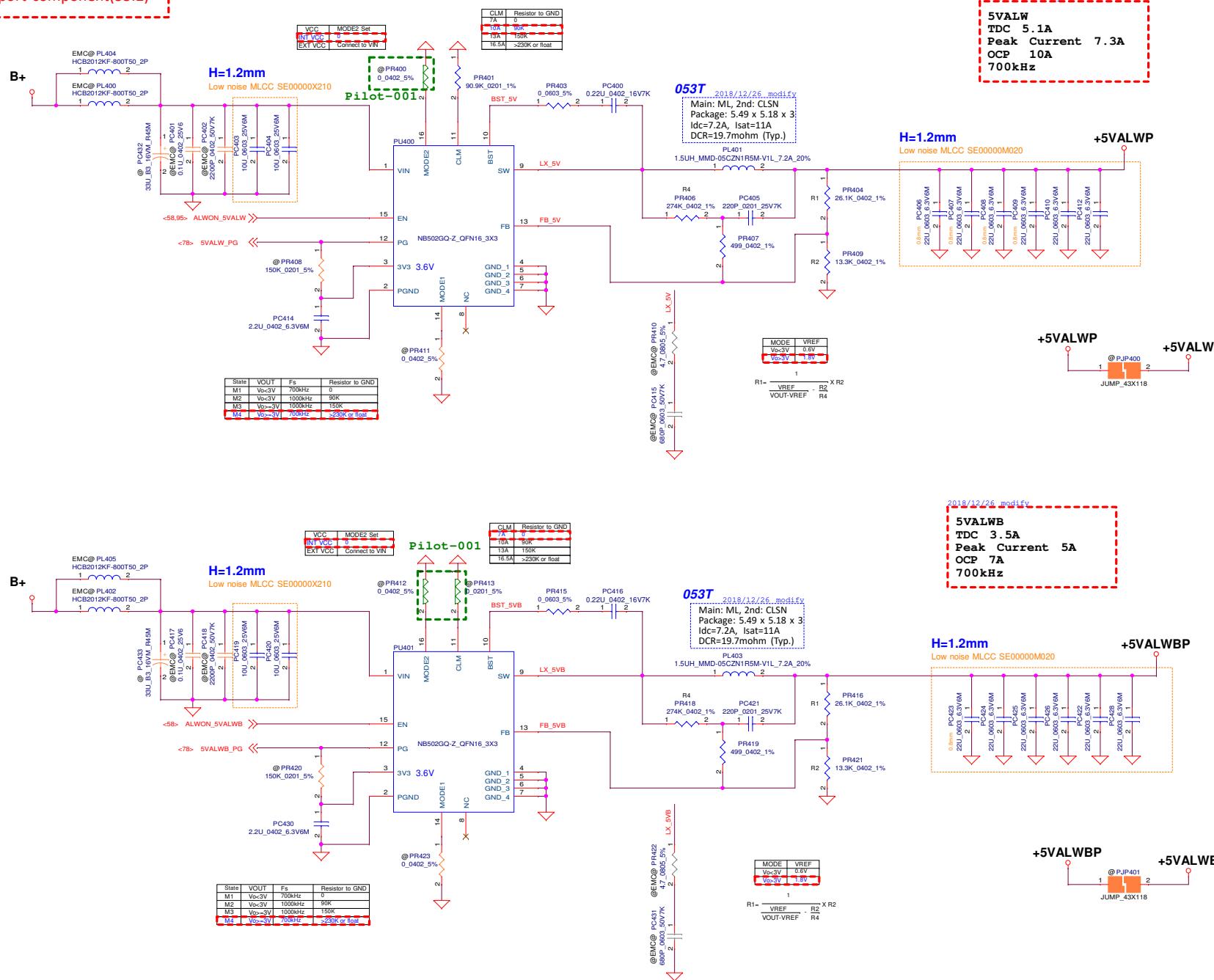


Controller(35.1), Support component(35.2)

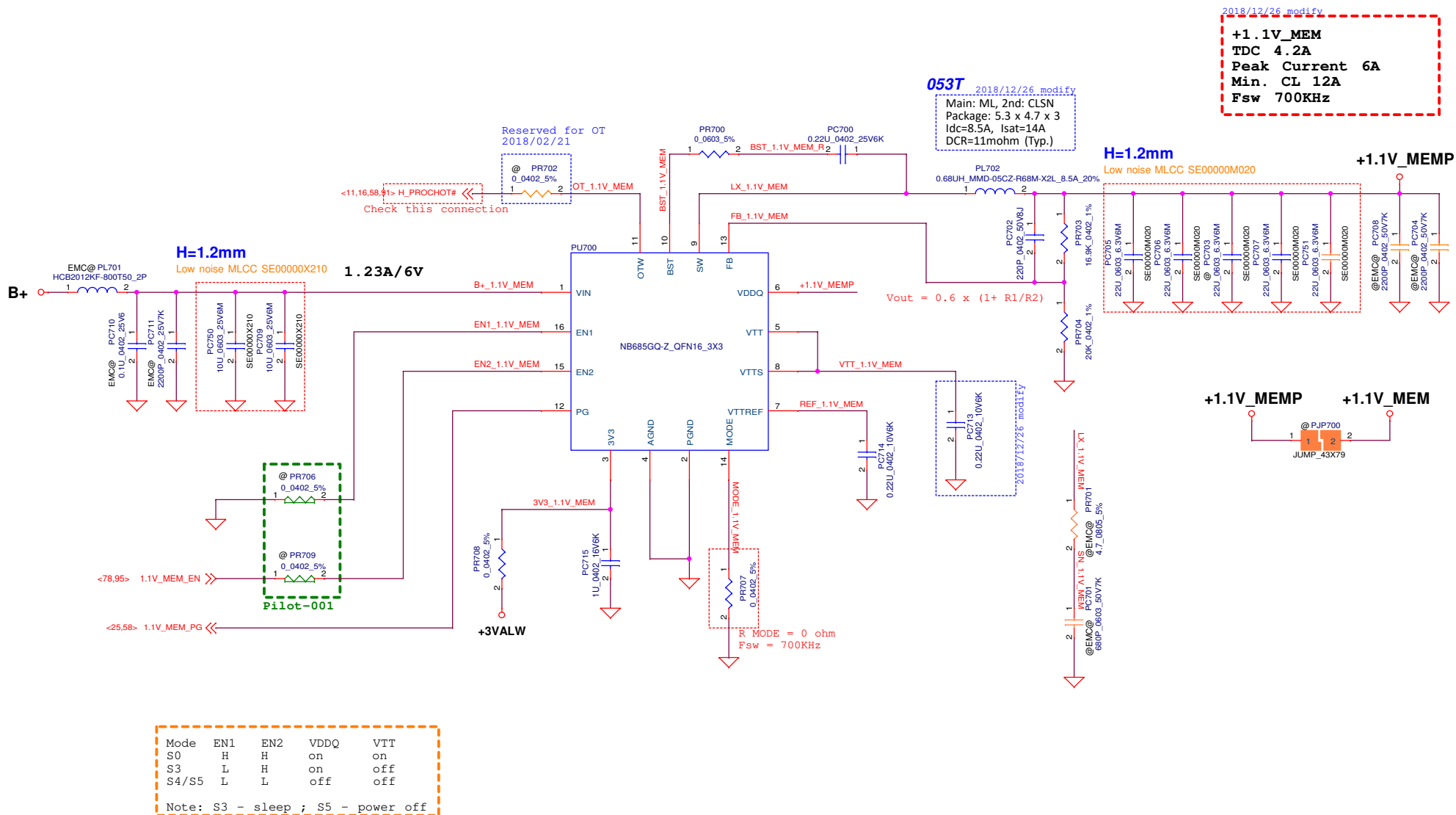


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR +3VALW</b>	
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				Document Number	0.4 (002)
				<b>LA-G172P</b> Date: Tuesday, December 24, 2019 Sheet 64 of 100	

# Controller(35.1), Support component(35.2)

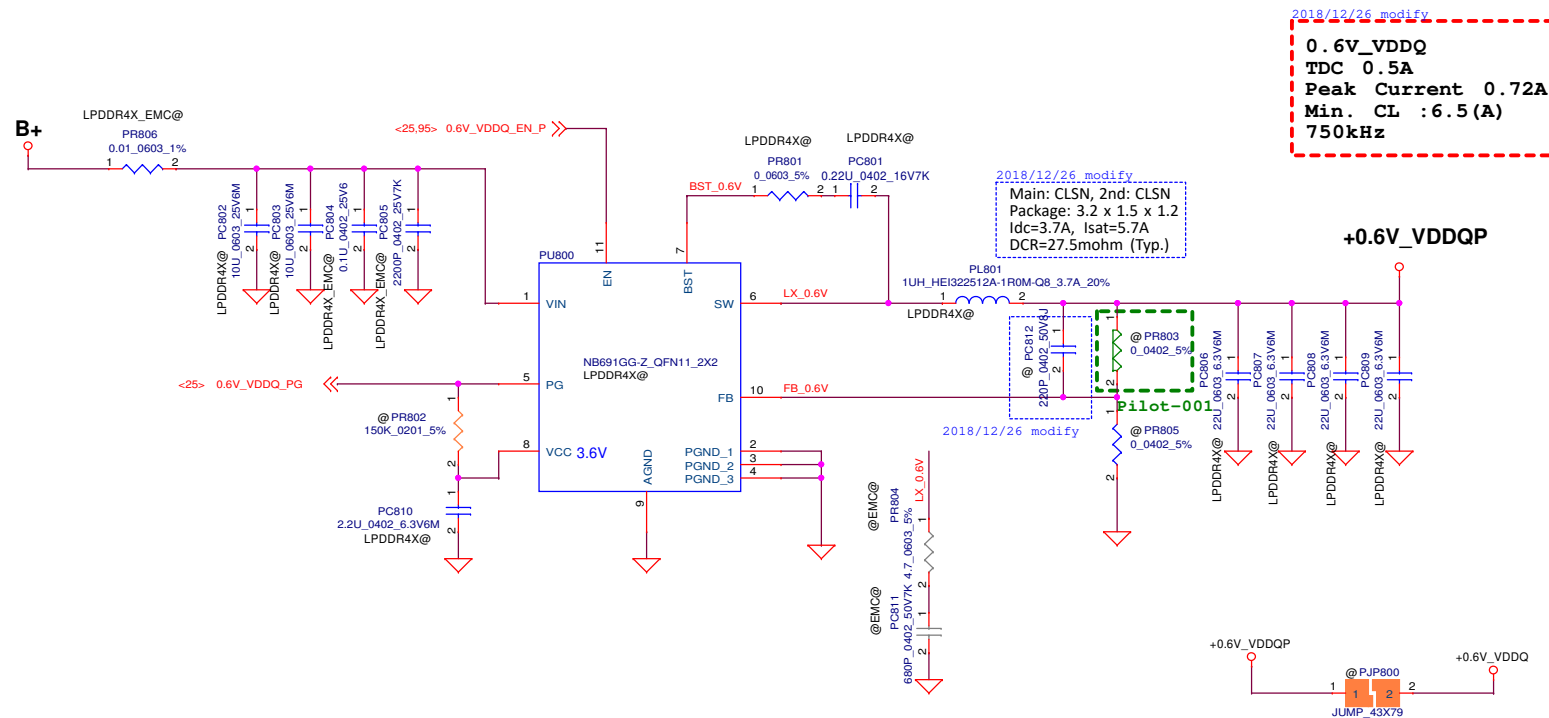


Controller(35.3), Support component(35.4)



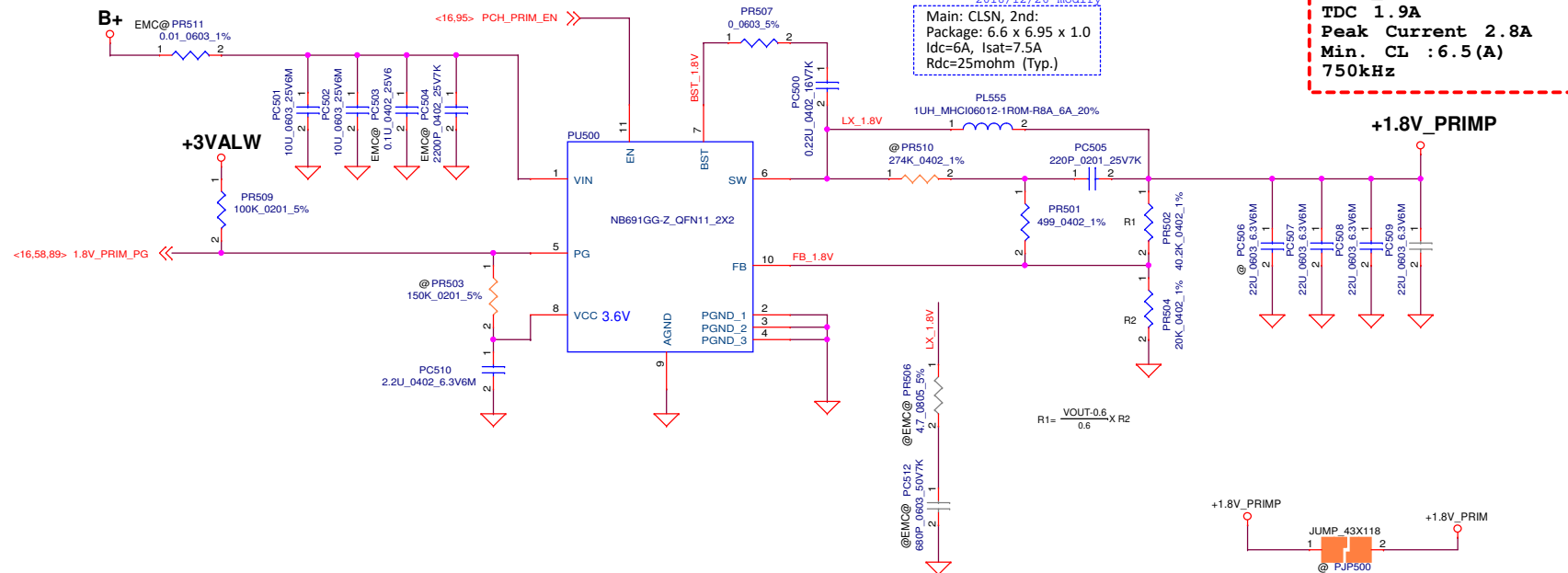
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Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title		
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				Size	Document Number	Rev
				<b>LA-G172P</b>		0.4 (X02)
				Date:	Tuesday, December 24, 2019	Sheet 86 of 100

Controller(35.3), Support component(35.4)



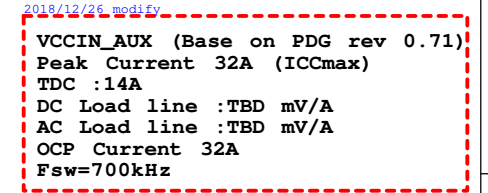
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Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title	PWR VDDQ4x
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Controller(35.13), Support component(35.14)



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					Size	Document Number	Rev		
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VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

State	CIM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

State	Interleaving	VID Down option	Resistor to GR
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

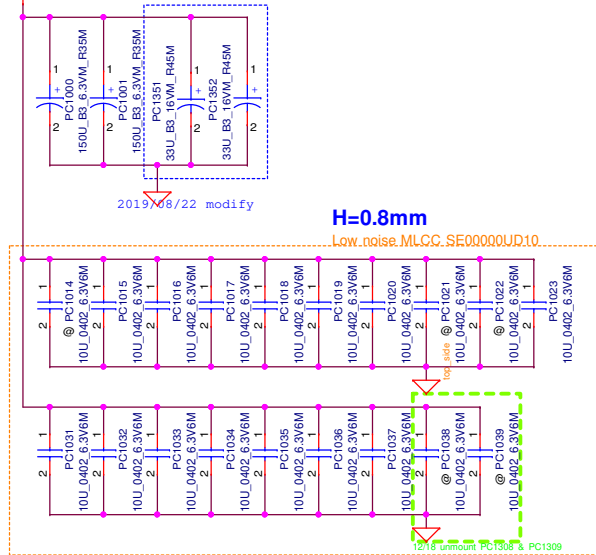
State	Fs (kHz)	Resistor to G
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

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					Size	Document Number	Rev		
					LA-G172P			0.4	(202)
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# Support component(36.4)

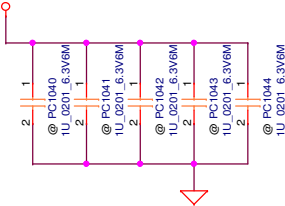
Primary side

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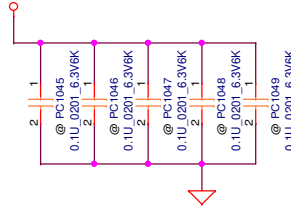


Backside

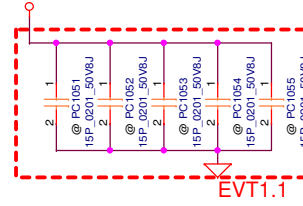
+VCCIN\_AUX



+VCCIN\_AUX



+VCCIN\_AUX

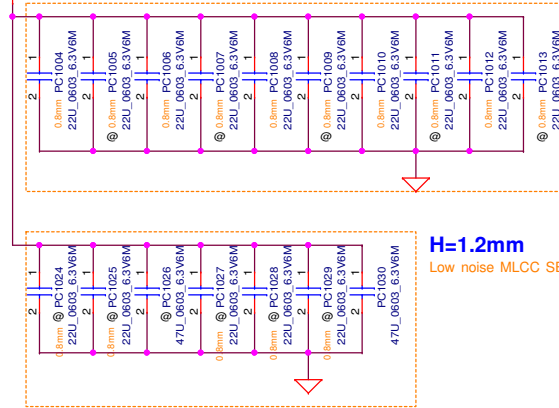


150U\_B3 \* 4 (POP\*2, NC\*2)  
10U\_0402 \* 19 (POP\*14, NC\*5)  
22U\_0603 \* 10 (POP\*1, NC\*9)  
47U\_0603 \* 7 (POP\*1, NC\*6)  
1U\_0201 \* 5 (NC\*5)  
0.1U\_0201 \* 5 (NC\*5)

PDG ver 1.1 Primary side:  
2x 330uF 7343  
3x 22uF 0603  
12x 10uF 0402  
1x 47uF 0805

+VCCIN\_AUX

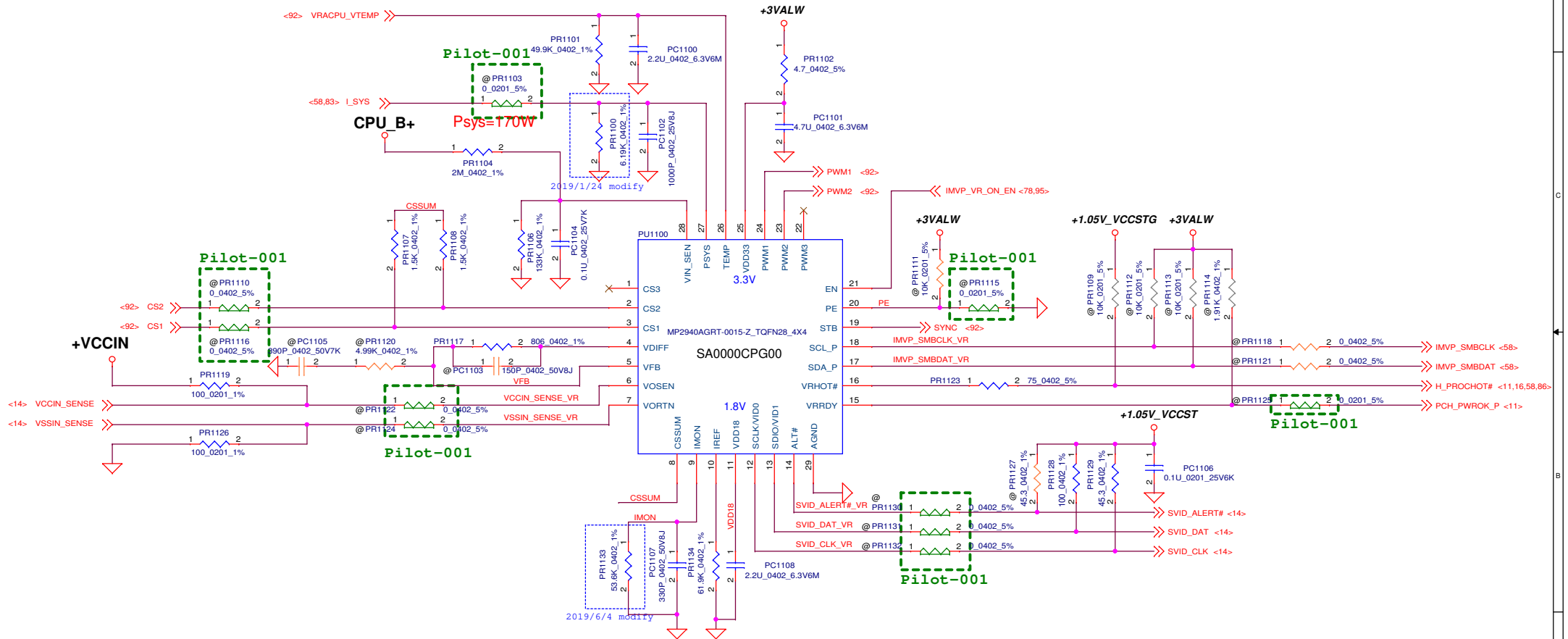
H=1.2mm  
Low noise MLCC SE00000M020



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Size	Document Number	Rev		0.4 (202)	
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Controller(36.1), Support component(36.3)

```
VCCIN (Base on PDG rev 0.71)
Peak Current 54A (ICCmax)
TDC :25A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz
```



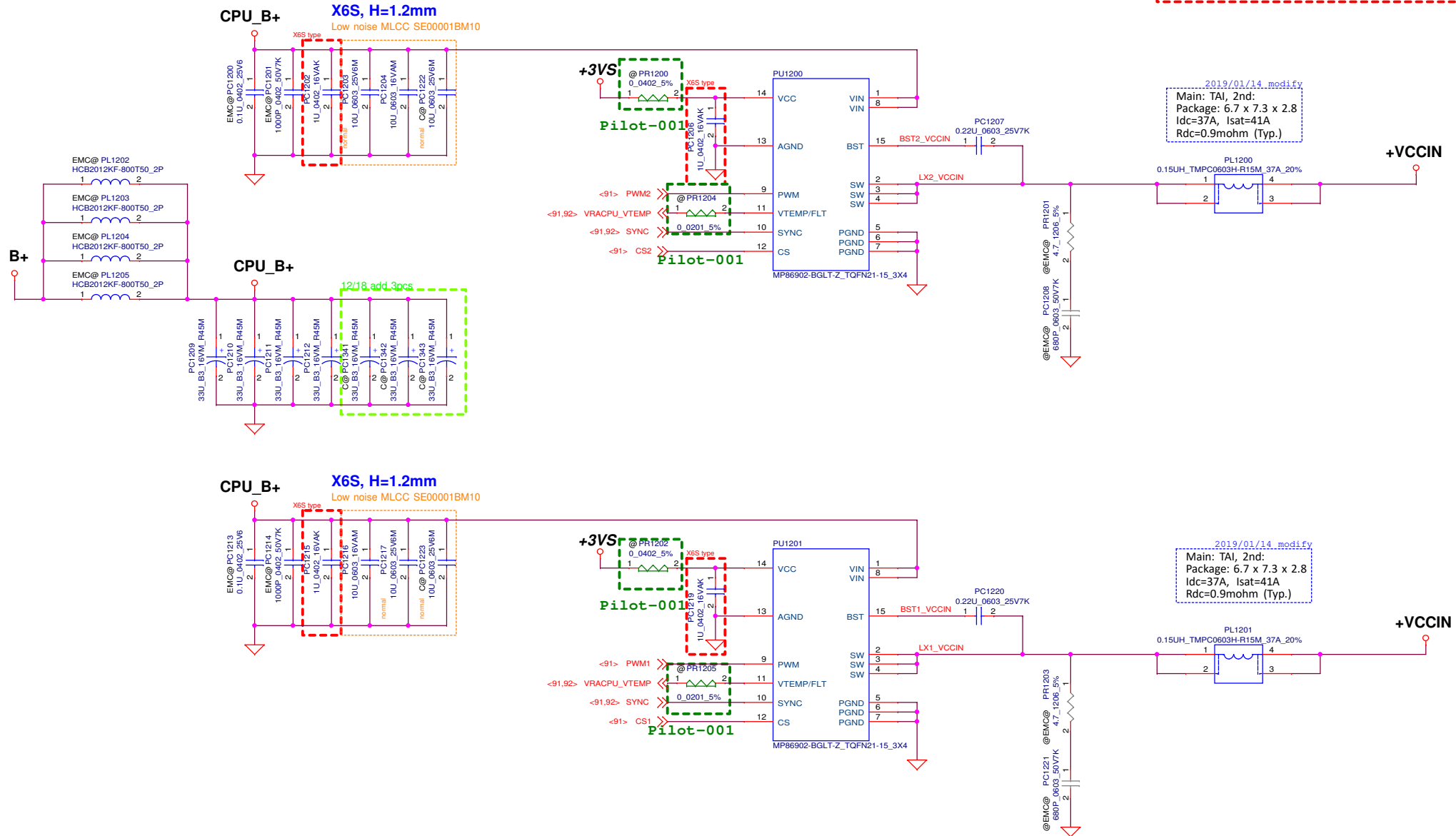
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Issued Date	2017/08/24	Deciphered Date	2017/08/24	Title	<b><i>PWR_VCCIN_CTRL</i></b>	
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Support component(36.2),(36.3)

```
VCCIN (Base on PDG rev 0.71)
Peak Current 62A (ICCmax)
PL2 TDC :36A
DC Load line :2mV/A
AC Load line :4mV/A
OCP Current TBDA
Fsw=800kHz
```

Main: TAI, 2nd:  
Package: 6.7 x 7.3 x 2.8  
Idc=37A, Isat=41A  
Rdc=0.9mohm (Typ.)

Main: TAI, 2nd:  
Package: 6.7 x 7.3 x 2.8  
Idc=37A, Isat=41A  
Rdc=0.9mohm (Typ.)

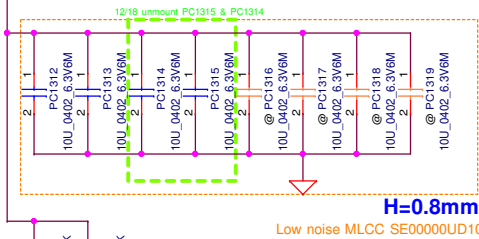
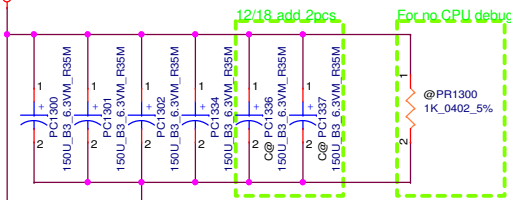


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					Size	Document Number	Rev
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					0.4 (202)		

# Support component(36.4)

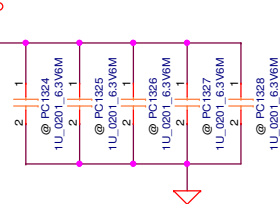
Primary side

+VCCIN

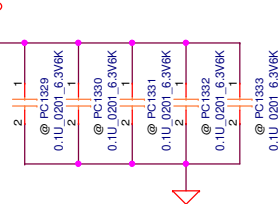


Backside

+VCCIN



+VCCIN



150U\_B3 \* 4 (pop\*2, NC\*2)  
10U\_0402 \* 8 (pop\*4, NC\*4)  
22U\_0603 \* 8 (pop\*7, NC\*1)  
47U\_0603 \* 2 (NC\*2)  
1U0402 \* 2  
1U\_0201 \* 5 (NC\*5)  
0.1U\_0201 \* 5 (NC\*5)

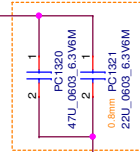
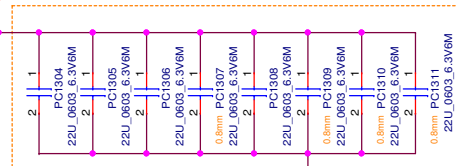
PDG ver 1.1 Primary side:

2x 1uF 0402  
4x 10uF 0402  
8x 22uF 0603  
1x 47uF 0805  
2x 330uF 7343

+VCCIN

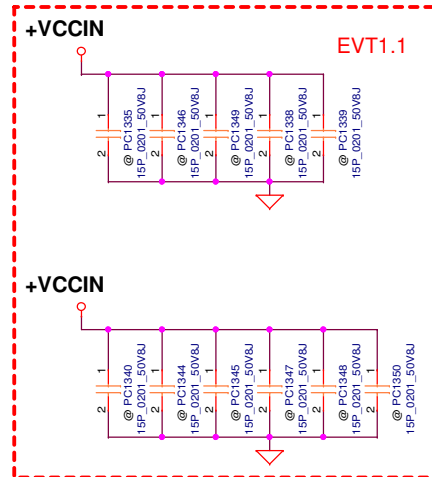
H=1.2mm

Low noise MLCC SE00000M020



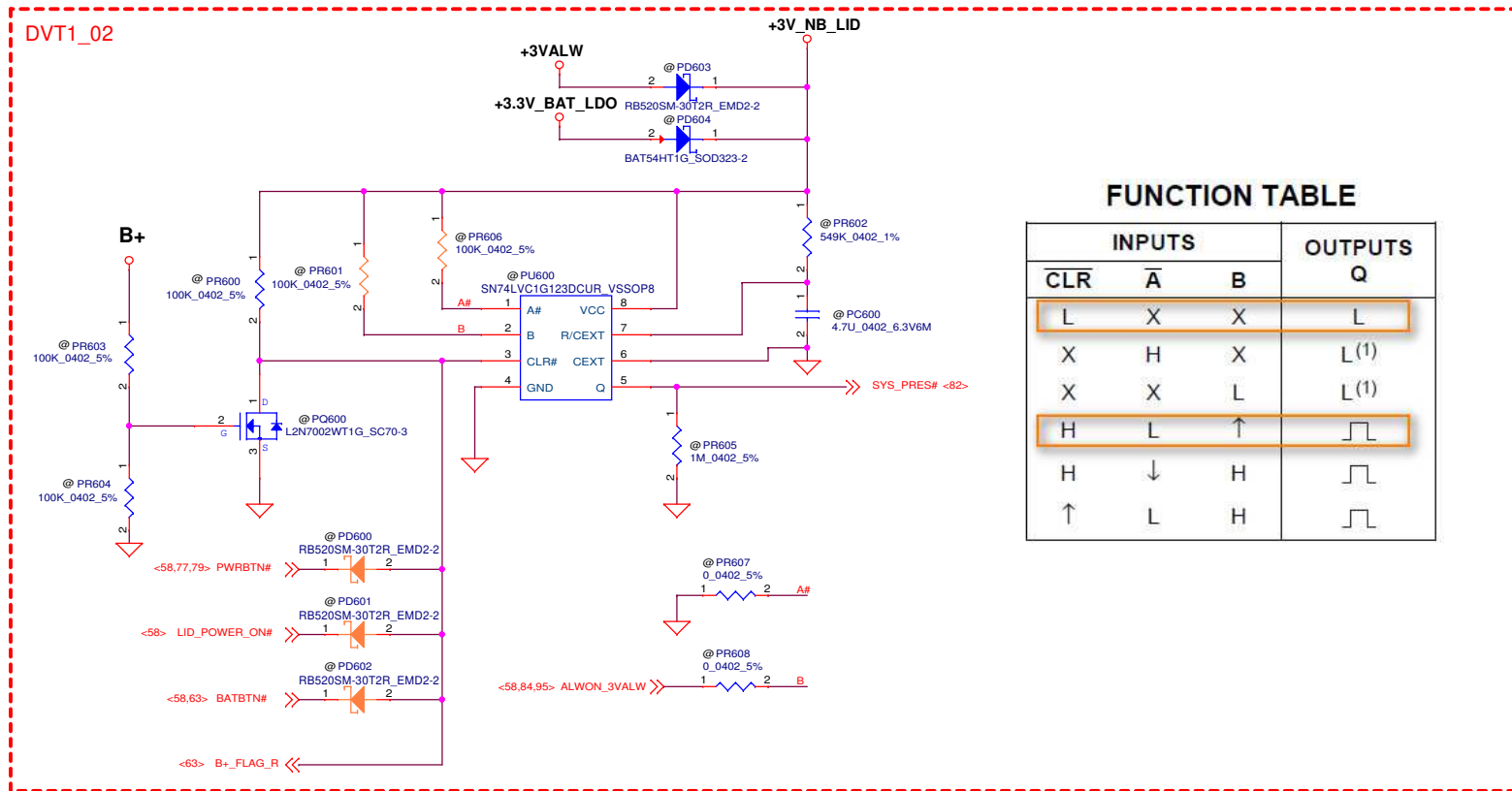
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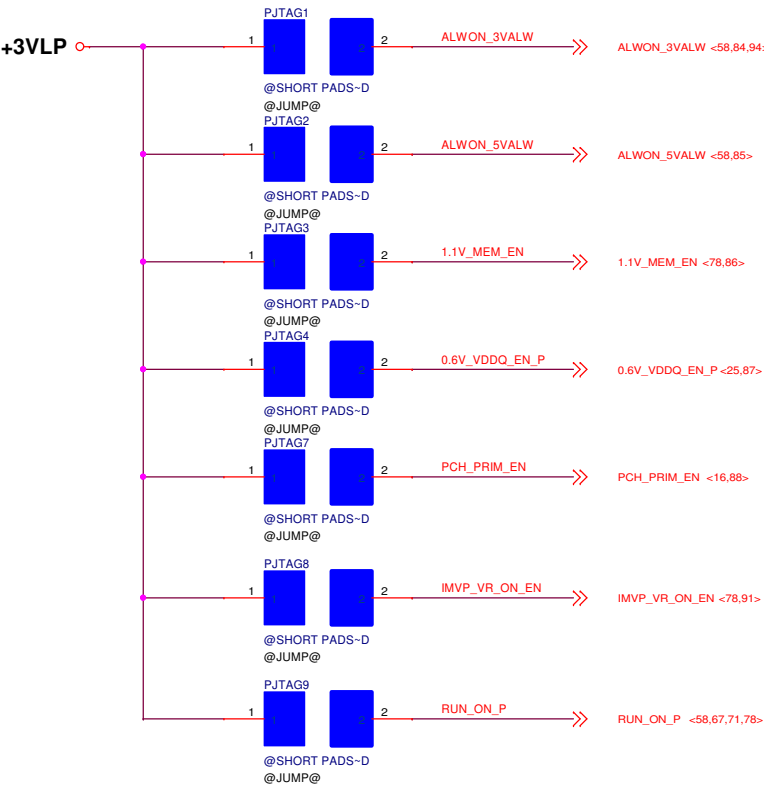
Low noise MLCC SE000015510



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Size		Document Number		Rev	
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Support component(37.1)

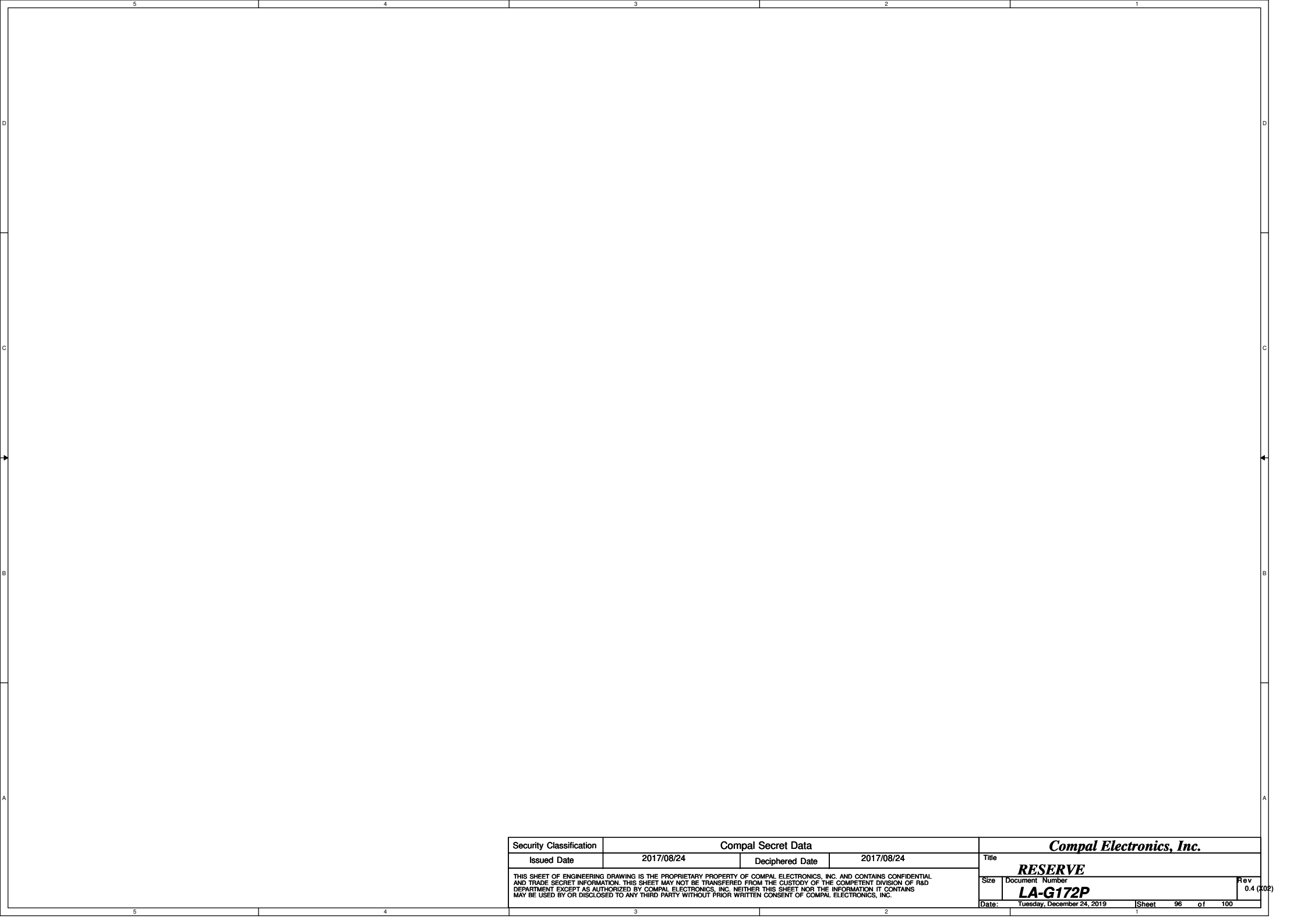




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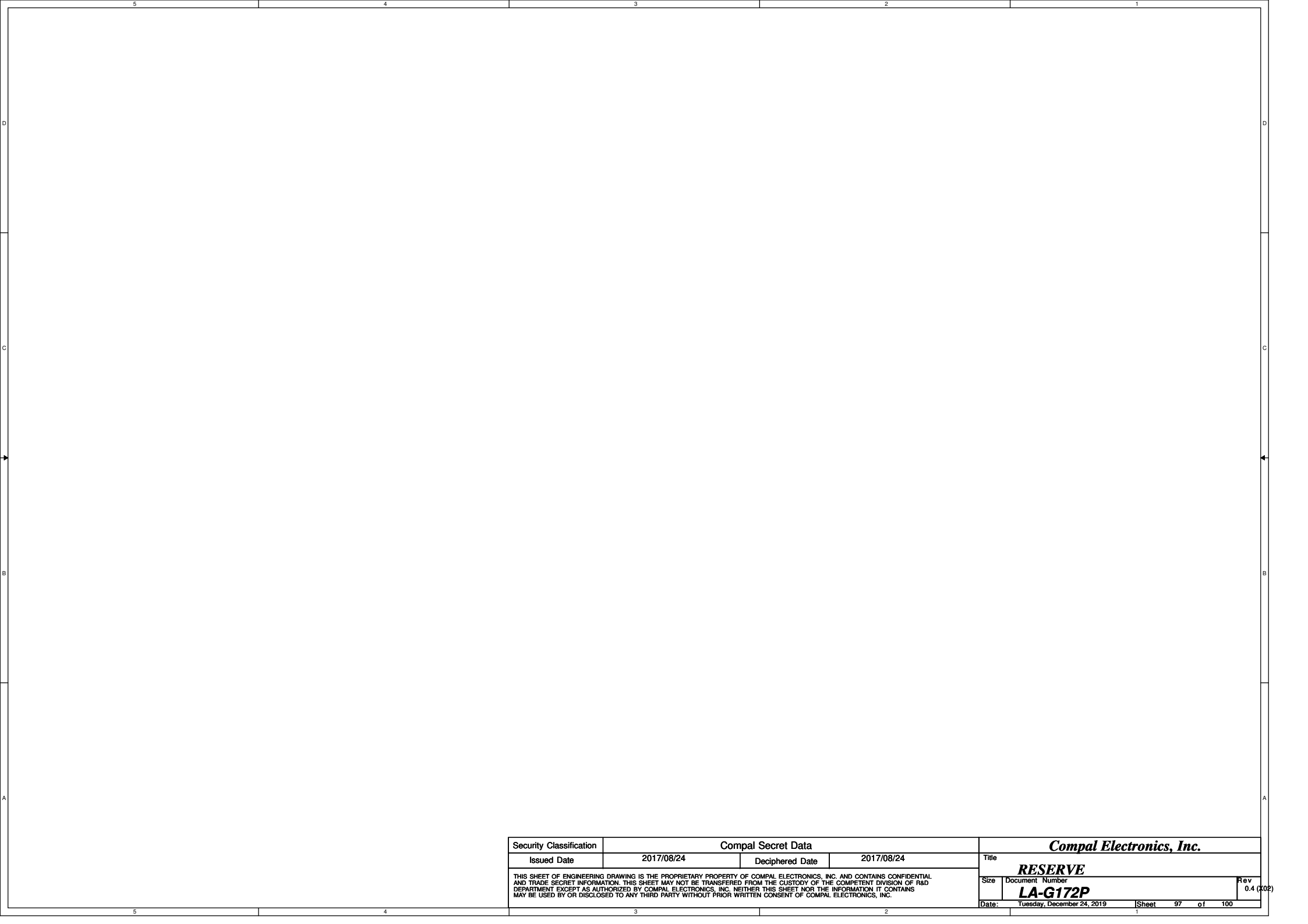
PWR Shortpads Debug

Rev 0.4 (202)

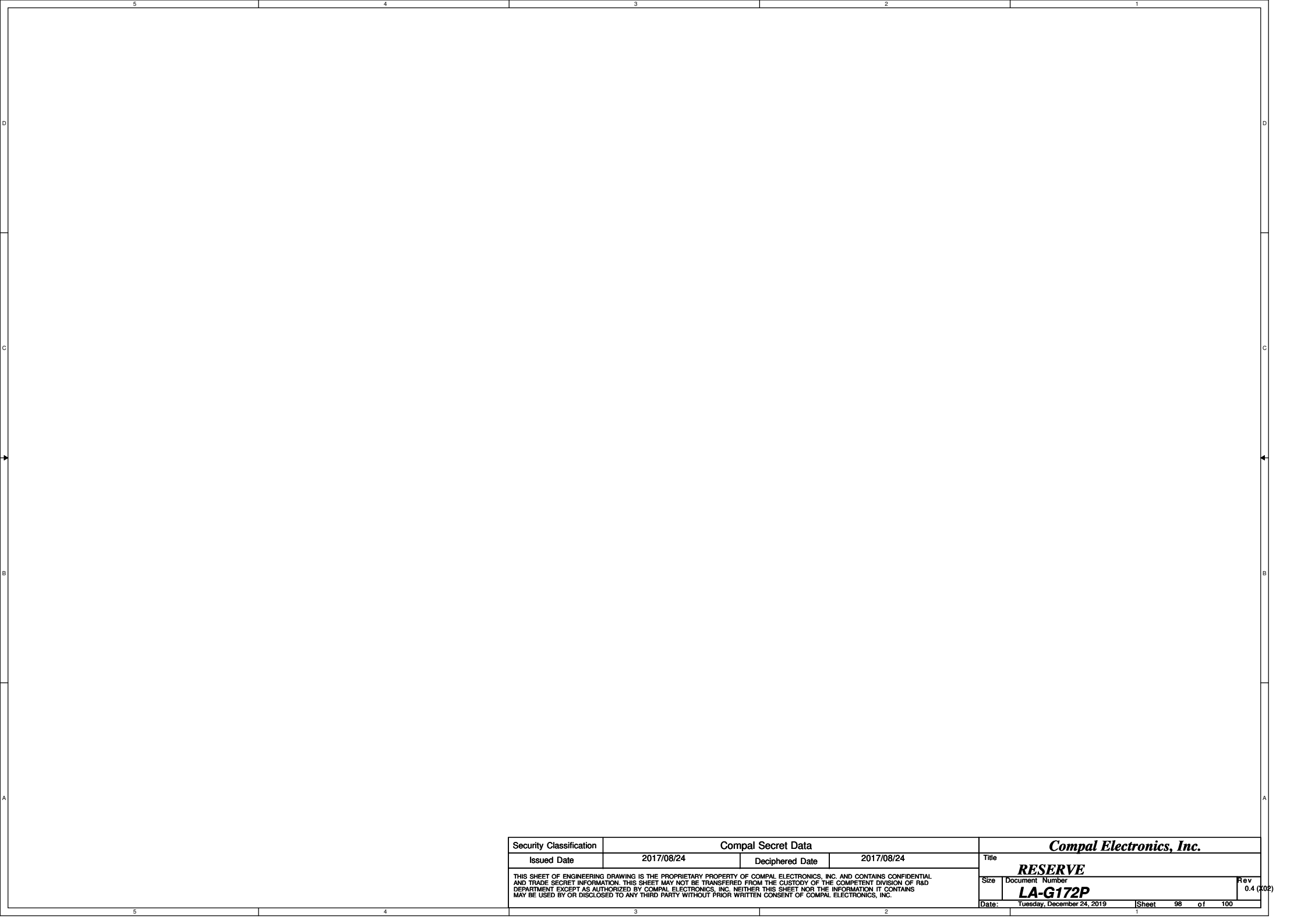


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